



CAYMET's
Siddhant College of Engineering
Academic Calendar
(A.Y. 2021-2022) Semester -I

Date:-03/08/2021

Sr. No	Activity	Proposed Dates
1.	Commencement of Teaching (TE & BE) (SEM-I).	15 th June 2021.
2.	Internal Academic & Administrative Audit.	Third week of June 2021.
3.	World Yoga Day Celebration [Online].	21 st June 2021.
4.	Bakri - Id (Id-Ul-Zua).	21 st July 2021.
5.	Independence Day.	15 th August 2021.
6.	Parsi New Year (Shahenshahi).	16 th August 2021.
7.	Moharum.	19 th August 2021.
8.	Commencement of Teaching (SE & ME II Year) (SEM-I).	20 th August 2021.
9.	IQAC Meeting - I [Online].	27 th August 2021.
10.	Departmental In-sem Exam (TE, BE & ME II Year) [Online MCQ's Type] -30 Marks.	Last week of August 2021.
11.	Declaration of Departmental In-sem Exam (TE, BE & ME- II Year) Result.	1 st September 2021.
12.	Celebration of SGI Foundation Day.	1 st September 2021.
13.	Celebration of Teachers Day.	5 th September 2021.
14.	Ganesh Chaturthi.	10 th September 2021.
15.	Celebration of Engineers Day.	15 th September 2021.
16.	Mahatma Gandhi Jayanti	2 nd October 2021.
17.	Commencement of FE & FE Induction programme (SEM-I).	First and Second week of October 2021.
18.	Department wise Prelim Exam (TE, BE & ME II Year) [Online MCQ's Type]-50 Marks.	First week of October 2021.
19.	Declaration of Departmental Prelim Exam Result.	11 th October 2021/22
20.	Department wise Practical Conduction of UG & PG [Online].	Second week of October 2021.
21.	Commencement of ME I Year. Induction programme of ME I Year & Direct Second Year students (SEM-I).	Second week of October 2021.
22.	End Term Submission (TE & BE).	Second week of October 2021.
23.	Dasara	15 th October 2021.
24.	Id-E-Milad.	19 th October 2021.
25.	End of Semester I (TE & BE).	20 th October 2021.
26.	Departmental In-sem Exam of FE, SE & ME I	Last week of October 2021.



	Year [Online MCQ's Type] -30 Marks.	
27.	Commencement of vacation for staff.	Last week of October 2021.
28.	SPPU Practical / Oral Examination (TE & BE) [Online]	Last week of October 2021.
29.	SPPU Theory Examination (TE & BE) [Online].	First week of November 2021.
30.	Declaration of Departmental In-sem Exam (FE, SE, ME- I & II Year) Result.	3 rd November 2021.
31.	Diwali Amavasaya – Lakshmi Pujan.	4 th November 2021.
32.	Diwali-Bali Pratipada	5 th November 2021.
33.	Diwali-Bhaubeej	6 th November 2021.
34.	Parent Teacher Meet [Online].	8 th November 2021.
35.	Department wise Prelim Exam (SE & ME II Year) [Online MCQ's Type]-50 Marks.	Second week of November 2021.
36.	End Term Submission (SE & ME II Year).	Second week of November 2021.
37.	End of Semester I (SE & ME II Year).	12 th November 2021.
38.	Declaration of Departmental Prelim Exam (SE & ME II Year) Result.	12 th November 2021.
39.	Gurunanak Jayanti.	19 th November 2021.
40.	IQAC Meeting – II [Online].	26 th November 2021.
41.	NAAC-AQAR Data filling for last academic year.	First week of December 2021.
42.	FE & ME I Year Prelim Exam [Online MCQ's Type]-50 Marks.	First week of December 2021.
43.	End Term Submission (FE & ME I Year) & Prelim Results.	Second week of December 2021.
44.	End of Semester I (FE & ME I Year).	10 th December 2021.
45.	SPPU Practical / Oral Examination (FE, SE, ME- I & II Year) [Online]	Third week of December 2021.
46.	Christmas.	25 th December 2021.
47.	SPPU Theory Examination (FE, SE, ME- I & II Year) [Online].	Last week of December 2021.

- Monthly Defaulter list-End of Every month during academic period.
- HOD Meeting with Faculty-Every Thursday.
- Principal Meeting with HoD-Every Friday.
- T&P activity-Every Thursday & Friday /as per the schedule given by T&P coordinator.
- NSS Activity-2 activities per semester.



Prof. *[Signature]* Shinde
Principal
Siddhant College of Engineering
Sudumbare, Pune - 412 108



CAYMET's
Siddhant College of Engineering
Academic Calendar
(A.Y. 2021-2022) Semester -II

Date:-28/12/2021


Sr. No	Activity	Proposed Dates
1.	Commencement of Teaching (TE & BE) (SEM-II).	15 th November 2021.
2.	Departmental In-sem Exam (TE & BE) [Online MCQ's Type] -30 Marks.	Last week of December 2021.
3.	Declaration of In-sem Exam Result (TE & BE).	3 rd January 2022.
4.	Commencement of Teaching (SE & ME II Year) (SEM-II).	3 rd January 2022.
5.	Commencement of (FE & ME I Year) and FE Induction programme (SEM-II).	Second week of January 2022.
6.	Republic Day.	26 th January 2022.
7.	College level SPPU Convocation Ceremony [Online].	First week of February 2022.
8.	E-Alumni Meet.	First week of February 2022.
9.	Chhatrapati Shivaji Maharaj Jayanti.	19 th February 2022.
10.	IQAC Meeting-III [Online].	25 th February 2022.
11.	Departmental In-sem Exam (FE, SE, ME I & II Year) [Online MCQ's Type] -30 Marks.	Last week of February 2022.
12.	Mahashivratri.	1 st March-2022.
13.	Declaration of In-sem Exam Result (FE, SE, ME I & II Year).	3 rd March 2022.
14.	Department wise Practical Conduction of UG & PG [Online].	Second week of March 2022.
15.	Holi [Second Day].	18 th March 2022.
16.	Gudhi Padwa	2 nd April 2022.
17.	Ram Navami.	10 th April 2022.
18.	Department wise Prelim Exam [Online MCQ's Type]-50 Marks (TE & BE).	Third week of April 2022.
19.	Dr. Babasaheb Ambedkar Jayanti.	14 th April 2022.
20.	Good Friday.	15 th April 2022.
21.	End Term Submission (TE & BE) & Prelim Results.	Last week of April 2022.
22.	Feedback Analysis [Online].	28 th April 2022.
23.	Parent Teacher Meet [Online].	29 th April 2022.
24.	End of Semester (TE & BE).	30 th April 2022.
25.	Maharashtra Din.	1 st May 2022.
26.	SPPU Practical / Oral Examination (TE & BE). [Online]	First Week of May 2022.



27.	Commencement of Remedial Classes [Online].	2 nd May 2022.
28.	Ramzan -Id [Id-Ul-Fitr].	3 rd May 2022.
29.	Department wise Prelim Exam [Online MCQ's Type]-50 Marks (FE,SE, ME I & II Year)	First week of May 2022.
30.	End Term Submission (FE, SE, ME I & II Year) & Prelim Results.	Second week of May 2022.
31.	SPPU Theory Examination (TE & BE) [Online].	Second week of May 2022.
32.	End of Semester (FE, SE, ME I & II Year).	15 th May 2022.
33.	Commencement of vacation for Staff.	15 th May 2022.
34.	Muddha Pourrama	16 th May 2022.
35.	SPPU Practical / Oral Examination (FE, SE, ME I & II Year) [Online].	Third week of May 2022.
36.	SPPU Theory Examination (FE, SE, ME I & II Year) [Online].	Last week of May 2022.
37.	IQAC Meeting-IV [Online].	27 th May 2022.
38.	Commencement of vacation for Students.	31 st May 2022.

- Monthly Defaulter list-End of Every month during academic period.
- HOD Meeting with Faculty-Every Thursday.
- Principal Meeting with HoD-Every Friday.
- T&P activity-Every Thursday & Friday /as per the schedule given by T&P coordinator.
- NSS Activity-2 activities per semester.




 Prof. U. V. Shinde
 Principal
 Siddhant College of Engineering
 Sudumbare, Pune - 412 109

CAMNET's
SIDDHANT COLLEGE OF ENGINEERING
DEPARTMENT OF MECHANICAL ENGINEERING
Department For Online Lecture - AY 2024-25, Semester - I, W. E. T. 20/10/2024

Day	Year & Div	09:30-10:30	10:30-11:30	11:30-12:30	12:30-01:30	01:30-02:30	02:30-03:30	03:30-04:30
Monday	SE - A	EMM(GGS)	SMAD (F1)	SM/SIB	Lunch Break	ETVSM	EEE (SRG)	HSM- Robotics/EV-PPG
	TE - A	NSM(PPG)	ELEC-I AFJP(BDG)	DME (Dr. PAM)		MTX (F2)	HT (SUD)	
Tuesday	BE - A	ELEC-I HVAC/FEA (VSM/SUD)	DOM(RRK)	H&P(GGS)	Lunch Break	ELEC-II AE/EAM (PPG/ F2)	CAD CAM(BBK)	HSM- Robotics/EV-PPG
	SE - A	EMM(GGS)	SMAD (F1)	SM/SIB		ETVSM	EEE(SRG)	
Wednesday	TE - A	NSM (PPG)	ELEC-I AFJP(BDG)	DME (Dr. PAM)	Lunch Break	MTX (F2)	HT (SUD)	HSM- Robotics/EV-PPG
	SE - A	EMM (GGS)	SMAD (F1)	SM/SIB		ETVSM	EEE (SRG)	
Thursday	BE - A	ELEC-I HVAC/FEA (VSM/SUD)	DOM(RRK)	H&P(GGS)	Lunch Break	ELEC-II AE/EAM (PPG/ F2)	CAD CAM (BBK)	HSM- Robotics/EV-PPG
	SE - A	EMM (GGS)	SMAD (F1)	SM/SIB		ETVSM	EEE (SRG)	
Friday	TE - A	NSM (PPG)	ELEC-I AFJP(BDG)	DME (Dr. PAM)	Lunch Break	MTX (F2)	HT (SUD)	HSM- Robotics/EV-PPG
	SE - A	EMM (GGS)	SMAD (F1)	SM/SIB		ETVSM	EEE (SRG)	

Project Work-I

Class, Teacher & Batch Wise GFM

Year - Div	Class	Batch	GFM	Batch	GFM	Batch	GFM
BE-A	SIB	A1	Prof. S.I. Bhargava	A2	Prof. G.G. Singh	A3	F2
TE-A	PPG	A1	Prof. P.P. Oshin	A2	Prof. B.D. Datta	A3	Prof. S.U. Deshpande
BE-A	VSM	A1	Prof. V.S. Murthy	A2	F1	A3	Prof. B.S. Soman

- # TE ELECTIVE E-1) Advanced Forming & Joining Processes
- # TE Honors & Minors: -
 - 1) Robotics
 - 2) Electric Vehicle
- # SE ELECTIVE E -
 - 1) Finite Element Analysis
 - 2) Heating Ventilation and Air Conditioning
- # BE ELECTIVE Ie -
 - 1) Automobile Engineering
 - 2) Energy Audit and Management

Departmental Time Table Exchange

HOD Mechanical

Principal

CABINET
STODOLANT COLLEGE OF ENGINEERING
DEPARTMENT OF MECHANICAL ENGINEERING
MASTER TIME TABLE (RECORDS) - H. 2023-24

DAY	CLASSIFY	Subject	Prereq	11:00-11:45	12:00-12:45	1:00-1:45	2:00-2:45	3:00-3:45	4:00-4:45
Monday	SE	AI (2024)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)
	TE	AI (2024)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)
Tuesday	SE	AI (2024)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)
	TE	AI (2024)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)
Wednesday	SE	AI (2024)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)
	TE	AI (2024)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)
Thursday	SE	AI (2024)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)
	TE	AI (2024)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)
Friday	SE	AI (2024)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)
	TE	AI (2024)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)	AI (1924)

CLASS	Section	CPM	QOS	Section	CPM	QOS	Section	CPM	QOS
SE	AI	AI	AI	AI	AI	AI	AI	AI	AI
TE	AI	AI	AI	AI	AI	AI	AI	AI	AI
SE	AI	AI	AI	AI	AI	AI	AI	AI	AI

[Signature]
 Dr. P. G. Gadekar & Pratik V. Chaudhary
 Departmental Time Table Incharge

[Signature]
 Dr. P. G. Gadekar
 HOD Mechanical

[Signature]
 Dr. B. A. Mhaswade
 Principal

Type	Class Teacher
SE (Class Room) (ET LAB)	Prof. G. D. Singh
TE (Class Room) (A-10)	Prof. B. D. Chitambar
SE (Class Room) (A-11)	Prof. S. D. Deshpande



SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE, PUNE

Department of Electronics & Telecommunication

Academic Year: 2021-2022

Semester: - VII

Class: BE (E & TC)

Class Teacher: Prof. A. A. Kokate

CLASS TIME TABLE

w.e.f.15/07/2021

DAY / TIME	8.45 - 9.45	9.45- 10.45	10.45 - 11.00	11.00- 12.00	12.00- 1.00	1.00- 1.30	1.30- 2.30	2.30- 3.30	3.30- 4.30
MON	CNS (SVP)	VLSI (AAK)	SHORT BREAK	EPD (NUK)	ERTOS (AVB)	LONG BREAK	RMT (VSB)	CNS(A1)(SVP)	
TUE	ERTOS (AVB)	CNS (SVP)		RMT (VSB)	EPD (NUK)		VLSI (AAK)	VLSI(A1)(AAK)	
WED	RMT (VSB)	EPD (NUK)		VLSI (AAK)	CNS (SVP)		ERTOS (AVB)	RMT(A1)(VSB)	
THU	RMT (VSB)	CNS (SVP)		VLSI (AAK)	ERTOS (AVB)		EPD (NUK)	ERTOS (A1)(AVB)	
FRI	VLSI (AAK)	CNS (SVP)		ERTOS (AVB)	RMT (VSB)		EPD (NUK)	TNP/INDUSTRIAL VISIT	

Theory		Practical/Tutorial		
Subject	Name of the Teacher	Subject	Name of the Laboratory	Name of the Teacher
EPD	NUK-Prof. N.U. Kure	ERTOS	SPECIALISATION LAB	AVB- Prof. Ashwini Bade
ERTOS	AVB- Prof. Ashwini Bade	CNS	RESEARCH SPECIALISATION LAB	SVP- Prof. S.V. Patil
CNS	SVP- Prof. S.V. Patil	RMT	INSTRUMENTATION LAB	VSB-- Prof. V.S. Bhatlawande
RMT	VSB-- Prof. V.S. Bhatlawande	VLSI	RESEARCH SPECIALIZATION LAB	AAK-Prof. A. A. Kokate
VLSI	AAK-Prof. A. A. Kokate			

Prof. Ashwini A. Kokate
TIME TABLE CO-ORDINATOR

Prof. Ashwini Bade
H.O.D (E&TC)

Prof. V. Shinde
PRINCIPAL



SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE, PUNE

Department of Electronics & Telecommunication
Academic Year: 2021-2022

Semester: -

III
Class: SE

Class Teacher: Prof. Prabhat Pallav

CLASS TIME TABLE
w.e.f. 15/07/2021

DAY / TIME	8.45 - 9.45	9.45- 10.45	10.45 - 11.00	11.00 - 1.00	1.00- 1.30	1.30- 2.30	2.30- 3.30	3.30- 4.30
MON	M-III (AT)	Elex-C (PP)	BREAK	Elex-C (A1)(PP)	BREAK	DC (NUK)	Elect-C ()	ESD ()
TUE	Elex-C (PP)	DC (NUK)		DS (A1)(VSB)		DS (VSB)	M-III (AT)	Elect-C ()
WED	DC (NUK)	Elex-C (PP)		Elect-C(A1) ()		DS (VSB)	Elect-C ()	M-III (AT)
THU	Elex-C (PP)	DS (VSB)		EMIT(A1)(AP)		Elect-C ()	M-III (AT)	ESD ()
FRI	Elect-C ()	DC (NUK)		DC(A1)(NUK)		DS (VSB)	Elex-C (PP)	M-III (AT)

Theory		Practical/Tutorial		
Subject	Name of the Teacher	Subject	Name of the Laboratory	Name of the Teacher
M-III	AT- Prof. A. Takale			
Elex-C	PP-Prof. Prabhat Pallav	DC	DE LAB	NUK - Prof. N. U. Kure
Elect-C		Elect-C	SSDC LAB	
DC	NUK - Prof. N. U. Kure	DS	Software LAB	VSB-- Prof. V.S. Bhatlawande
DS	VSB-- Prof. V.S. Bhatlawande	Elex-C	BASIC ELECTRIC LAB	
ESD		ESD	INSTRUMENTATION LAB	

Prof. Ashwini A. Kokate
TIME TABLE CO-ORDINATOR

Prof. Ashwini Bada
H.O.D (E&TC)

Prof. V. Shinde
PRINCIPAL



SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE, PUNE

Department of Electronics & Telecommunication

Academic Year: 2021-2022

Semester: - V

Class: TE

Class Teacher: Prof. N. U. Kure

CLASS TIME TABLE

w.e.t. 15/07/2021

DAY / TIME	8.45 - 9.45	9.45- 10.45	10.45 - 11.00	11.00 - 1.00	1.00- 1.30	1.30- 2.30	2.30- 3.30	3.30- 4.30
MON	CN (PP)	EFT (NUK)	SHORT BREAK	DSP(A1)(AAK)	LONG BREAK	MC (AVB)	DBMS (AAK)	DC (SVP)
TUE	DBMS (AAK)	CN (PP)		ESD(A1)(NSK)		MECT(A1)(AVB)	EFT (NUK)	
WED	DC (SVP)	MC (AVB)		MC(A1)(AVB)		EFT (NUK)	CN (PP)	DBMS (AAK)
THU	EFT (NUK)	DBMS (AAK)		EMTL(A1)(NUK)		MC (AVB)	DC (SVP)	CN (PP)
FRI	EFT (NUK)	MC (AVB)		DC(A1)(SVP)		DBMS (AAK)	DC (SVP)	SD

Theory		Practical/Tutorial		
Subject	Name of the Teacher	Subject	Name of the laboratory	Name of the Teacher
EFT	NUK - Prof. N. U. Kure	CN	SPECIALIZATION LAB	PP-Prof. Prabhat Pallav
MC	AVB -Prof. A. V. Bade	MC	MCA LAB	AVB -Prof. A. V. Bade
DC	SVP- Prof. S.V. Patil	DC	COMN LAB	SVP- Prof. S.V. Patil
DBMS	AAK- Prof A. A. Kokate	DBMS	RESEARCH SPECIALIZATION LAB	AAK- Prof. A. A. Kokate
CN	PP-Prof. Prabhat Pallav	EMTL	B. ELECTRICAL LAB	NUK - Prof. N. U. Kure
SD				

Prof. Ashwini A. Kokate
TIME TABLE CO-ORDINATOR

Prof. Ashwini Bade
H.O.D (E&TC)

Prof. V. V. Shinde
PRINCIPAL



SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE, PUNE

Department of Electronics & Telecommunication

Academic Year: 2021-2022

Semester: - I

Class: ME FE (VLSI & EMBEDDED SYSTEMS)

Class Teacher: Prof. M.U Inamdar

CLASS TIME TABLE

w.e.f. 1/08/2021

DAY / TIME	8.30 - 9.25	9.25- 10:20	10:20 - 10.50	10.50- 11.45	11.45- 12.40	12.40- 1.30	1.30- 2.25	2.25-3.20	3.20- 4.15
MON	RM (SVP)		SHORT BREAK	RM (SVP)	WSN (VSB)	LONG BREAK		RM(A1)(SVP)	
TUE	RM (SVP)	D-CMOS (JRP)		WSN (VSB)	ESD (AVB)		D-CMOS (JRP)	D-CMOS(A1)(JRP)	
WED	RC (NSK)	RC (NSK)		ESD (AVB)	D-CMOS (JRP)		RM (SVP)	RC(A1)(NSK)	
THU	WSN (VSB)	WSN (VSB)		D-CMOS (JRP)	RC (NSK)		WSN (A1)(VSB)		
FRI	ESD (AVB)	ESD (AVB)		RC (NSK)			ESD(A1)(AVB)		WSN (VSB)

Theory		Practical/Tutorial		
Subject	Name of the Teacher	Subject	Name of the Laboratory	Name of the Teacher
RC	NSK- Prof. N.S. Kulkarni	RC	RESEARCH SPECIALIZATION LAB	NSK- Prof. N.S. Kulkarni
WSN	VSB- Prof. V.S. Bhatlawande	WSN	SPECIALIZATION LAB	VSB- Prof. V.S. Bhatlawande
ESD	AVB - Prof. A. V. Bade	ESD	MCA LAB	AVB - Prof. A. V. Bade
RM	SVP- Prof. S.V. Patil	RM	RESEARCH SPECIALIZATION LAB	SVP- Prof. S.V. Patil
D-CMOS	JRP- DR. J. R. Panchal	D-CMOS	RESEARCH SPECIALIZATION LAB	JRP- DR. J. R. Panchal

Prof. Ashwini A. Kokate
TIME TABLE CO-ORDINATOR

[Signature]
Prof. Ashwini Bade
H.O.D (E&TC)

[Signature]
Prof. U.V. Shinde
PRINCIPAL



CLASS TIME TABLE

w.e.f. 1/8/2021

DAY / TIME	8.30 - 9.25	9.25- 10:20	10:20 - 10.50	10.50- 11.45	11.45- 12.40	12.40 -1.30	1.30- 2.25	2.25- 3.20	3.20- 4.15
MON			SHORT BREAK			LONG BREAK			
TUE									
WED									
THU	TVVC (AAK)	ELCT-III(VSB)		ELCT-III(VSB)	TVVC (AAK)		SEM-II	TVVC(A1)(AAK)	
FRI	ASIC (NSK)	ASIC (NSK)		TVVC (AAK)	TVVC (AAK)		SEM-II	ASIC(A1)(NSK)	
SAT	ELCT-III(VSB)	ELCT-III(VSB)		ASIC (NSK)	ASIC (NSK)		ELCT-III(A1)(VSB)		

Theory		Practical/Tutorial		
Subject	Name of the Teacher	Subject	Name of the Laboratory	Name of the Teacher
ELCT-III	VSB- Prof. V.S. Bhatlawande	ELCT-III	RESEARCH SPECIALIZATION LAB	VSB- Prof. V.S. Bhatlawande
ASIC	NSK- Prof. N.S. Kulkarni	ASIC	RESEARCH SPECIALIZATION LAB	NSK- Prof. N.S. Kulkarni
TVVC	AAK- Prof A. A. Kokate	TVVC	RESEARCH SPECIALIZATION LAB	AAK- Prof A. A. Kokate

Prof. Ashwini A. Kokate
TIME TABLE CO-ORDINATOR

Prof. Ashwini Bade
H.O.D (E&TC)

Prof. U.V. Shinde
PRINCIPAL

GANNETT'S
SIDDHANT COLLEGE OF ENGINEERING, SIDDHAPUR POUDALIM
DEPARTMENT OF AEC, THIRUVARUR
MASTER TIMETABLE

DAY / TIME	MONDAY										TUESDAY										WEDNESDAY										THURSDAY										FRIDAY									
	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II															
08:00-09:00	SS I (SBD)	CN (GAA)	BOS (PT)	SOC (NLUK)		CS (SVS)	FM (GAA)	MC I (GAA)	SOC (NLUK)		SS I (SBD)	POC (NLUK)	MC (GAA)		CS (SVS)	POC (NLUK)	MC (GAA)	ACMOS (AVB)		SS I (SBD)	POC (NLUK)	MC (GAA)		CS (SVS)	POC (NLUK)	MC (GAA)	ACMOS (AVB)		SS I (SBD)	POC (NLUK)	MC (GAA)		CS (SVS)	POC (NLUK)	MC (GAA)	ACMOS (AVB)														
09:00-10:00	POCS (KAK)	EP (AVB)	WSM (SBD)	ACMOS (AVB)		ESD (SVS)	EP (AVB)	WTR (SBD)	ACMOS (AVB)		POCS (KAK)	POC (NLUK)	MC (GAA)		ESD (SVS)	POC (NLUK)	MC (GAA)			POCS (KAK)	POC (NLUK)	MC (GAA)		ESD (SVS)	POC (NLUK)	MC (GAA)		POCS (KAK)	POC (NLUK)	MC (GAA)		ESD (SVS)	POC (NLUK)	MC (GAA)																
10:00-11:00	CS (SVS)	PDC (NLUK)	AVE (VSB)			POCS (KAK)	POC (NLUK)	BOS (PF)	EAS (VSB)		CS (SVS)	POC (NLUK)	BOS (PF)	EAS (VSB)		CS (SVS)	POC (NLUK)	BOS (PF)	EAS (VSB)		CS (SVS)	POC (NLUK)	BOS (PF)	EAS (VSB)		CS (SVS)	POC (NLUK)	BOS (PF)	EAS (VSB)		CS (SVS)	POC (NLUK)	BOS (PF)	EAS (VSB)																
11:00-12:00	ESD (SVS)	EP (AVB)	MAC (GAA)	EAS (VSB)		ESD (SVS)	CN (GAA)	AVE (VSB)			ESD (SVS)	CN (GAA)	AVE (VSB)		ESD (SVS)	CN (GAA)	AVE (VSB)			ESD (SVS)	CN (GAA)	AVE (VSB)		ESD (SVS)	CN (GAA)	AVE (VSB)		ESD (SVS)	CN (GAA)	AVE (VSB)		ESD (SVS)	CN (GAA)	AVE (VSB)																
12:00-1:30	SS I (SBD)	EP (AVB)	BOS (PF)	SOC (NLUK)		PBL (NLUK)	POC (NLUK)	BOS (PF)			PBL (NLUK)	POC (NLUK)	BOS (PF)		PBL (NLUK)	POC (NLUK)	BOS (PF)			PBL (NLUK)	POC (NLUK)	BOS (PF)		PBL (NLUK)	POC (NLUK)	BOS (PF)		PBL (NLUK)	POC (NLUK)	BOS (PF)		PBL (NLUK)	POC (NLUK)	BOS (PF)																
1:30-2:30	SS I (SBD)	TNP (VSB)	AVE (VSB)	EPD (PF)		PBL (NLUK)	POC (NLUK)	PS2			PBL (NLUK)	POC (NLUK)	PS2		PBL (NLUK)	POC (NLUK)	PS2			PBL (NLUK)	POC (NLUK)	PS2		PBL (NLUK)	POC (NLUK)	PS2		PBL (NLUK)	POC (NLUK)	PS2		PBL (NLUK)	POC (NLUK)	PS2																
2:30-3:30	SS I (SBD)	TNP (VSB)	PS2			PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)		PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)		PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)		PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)		PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)		PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)																
3:30-4:30	SS I (SBD)	TNP (VSB)	PS2			PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)		PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)		PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)		PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)		PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)		PBL (NLUK)	POC (NLUK)	LIB	EPD (PF)																

LUNCH BREAK

SHORT BREAK

Time Table In-charge
Prof. Kalyani Kandan

Time Table Coordinator
Prof. Kalyani Kandan

BOB
Prof. Prabhakar Pethav

Dr. Rajesh Kumar

CADDET
SIDDHANT COLLEGE OF ENGINEERING, SIDDHANT PUNE-411007
DEPARTMENT OF AEC, ENGINEERING
MATTER TIME-TABLE
A.Y. 2022-23

MATTER	MONDAY					TUESDAY					WEDNESDAY					THURSDAY					FRIDAY									
	SE	TE	ME	ME I	ME II	SE	TE	ME	ME I	ME II	SE	TE	ME	ME I	ME II	SE	TE	ME	ME I	ME II	SE	TE	ME	ME I	ME II	SE	TE	ME	ME I	ME II
11:00-11:30																														
11:30-12:00																														
12:00-12:30																														
12:30-1:00																														
1:00-1:30																														
1:30-2:00																														
2:00-2:30																														
2:30-3:00																														
3:00-3:30																														

Time Table-charge
 Prof. Kalyani Kadam

Time Table C Coordinator
 Prof. Kalyani Kadam

HOOD
 Prof. Prashant Patil

Dr. Kishu Khadke

CAMLET'S
SIDDHANT COLLEGE OF ENGINEERING, SIROMBAHE POSE-412308
DEPARTMENT OF JEEC, INDIA
MASTER TIME-TABLE

DAY/TIME	MONDAY					TUESDAY					WEDNESDAY					THURSDAY					FRIDAY							
	SE	TE	BE	MOR I	MOR II	SE	TE	BE	MOR I	MOR II	SE	TE	BE	MOR I	MOR II	SE	TE	BE	MOR I	MOR II	SE	TE	BE					
08:00 - 09:00																												
09:00 - 10:00																												
10:00 - 11:00																												
11:00 - 12:00																												
12:00 - 13:00																												
13:00 - 14:00																												
14:00 - 15:00																												
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16:00 - 17:00																												
17:00 - 18:00																												
18:00 - 19:00																												
19:00 - 20:00																												
20:00 - 21:00																												
21:00 - 22:00																												
22:00 - 23:00																												
23:00 - 24:00																												

Time Table In-charge
Prof. Kalyani Kadam

Time Table Coordinator
Prof. Kalyani Kadam

Prof. Prakash Patil

Principal
Dr. Rajesh Khambhage

CATHERY'S
HERBERT COLLEGE OF ENGINEERING, SRIRANGAPET
Established in 1974, ISO 9001:2015 Certified
MAINTENANCE TIME TABLE

DAY/TIME	MONDAY				TUESDAY				WEDNESDAY				THURSDAY				FRIDAY									
	SE	TR	BE	MR I	MR II	SE	TR	BE	MR I	MR II	SE	TR	BE	MR I	MR II	SE	TR	BE	MR I	MR II	SE	TR	BE	MR I	MR II	
10:00-11:00				SOC (ONLINE)					SOC (ONLINE)																	
11:00-12:00																										
12:00-13:00																										
13:00-14:00																										
14:00-15:00				SOC (ONLINE)																						
15:00-16:00																										
16:00-17:00																										
17:00-18:00																										

This Table is charge
 Prof. Kalyani Kadam

This Table Coordinator
 Prof. Kalyani Kadam

Prof. P. Mahan Velar

Approved
 Dr. Bimal Khanna

CAVIERI'S
ASSOCIATE COLLEGE OF ENGINEERING, TECHNOLOGICAL PROGRESS
 UNIVERSITY OF APJS, PONDICHERRY
MASTER TIME TABLE

DAY/TIME	SEMESTER I					SEMESTER II					SEMESTER III					SEMESTER IV									
	SE	TE	BE	ME I	ME E	SE	TE	BE	ME I	ME E	SE	TE	BE	ME I	ME E	SE	TE	BE	ME I	ME E	SE	TE	BE		
08:00-09:00																									
09:00-10:00																									
10:00-11:00																									
11:00-12:00																									
12:00-01:00																									
01:00-02:00																									
02:00-03:00																									
03:00-04:00																									
04:00-05:00																									
05:00-06:00																									

[Signature]
 This Table is charge
 Prof. Kalyani Kandan

[Signature]
 This Table Coordinator
 Prof. Kalyani Kandan

[Signature]
 Prof. Kalyani Kandan

[Signature]
 Principal
 Dr. K. S. K. K.

CAVAYET'S
SIDDHANT COLLEGE OF ENGINEERING, SIDDHANT PUNE-411109
DEPARTMENT OF EATC, ENGINEERING
MASTER TIME TABLE

Name Of Staff: **Prof. Swati Deshmukh**
 A.Y - 2023-22

SEM II

WITH EFFECT FROM

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY			
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	
8:45 - 9:45	SS I (SBD)						SS I (SBD)						W/SN (SBD)	SS I (SBD)		
9:45 - 10:45			W/SN (SBD)													
10:45 - 11:00	SHORT BREAK															
11:00 - 12:00														DAL		
12:00 - 01:00							TRINI PROJ CT			DAL	TRINI PROJ CT			DAL	TRINI PROJ CT	
1:00 - 1:30	LUNCH BREAK															
1:30 - 2:30	SS I (SBD)															
2:30 - 3:30	SS I (SBD)															
3:30 - 4:30	SS I (SBD)															

[Signature]
 Time Table In-charge
 Prof. Kalyani Kadam

[Signature]
 Time table Coordinator
 Prof. Kalyani Kadam

[Signature]
 Prof. Parthab Patil

[Signature]
 Principal
 Dr. Rahul Khandagale

CAVNET'S
SIDDHANT COLLEGE OF ENGINEERING, SIDDHAPUR PUNE-412109
 DEPARTMENT OF EMTC ENGINEERING
MASTER TIME-TABLE

Name Of Staff: Prof. Kalyani Kadam
 A.Y.-2021-22

SEM II
 WITH EFFECT FROM

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY			
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	
8:45 - 9:45					PM (KAK)											
9:45 - 10:45	POCS (KAK)															
10:45 - 11:00	SHORT BREAK															
11:00 - 12:00				POCS (KAK)												
12:00 - 01:00							MINI PROJ CT			POCS (KAK) DAL		MINI PROJ CT		DAL	PM (KAK) MINI PROJ CT	
1:00 - 1:30	LUNCH BREAK															
1:30 - 2:30										POCS (KAK)						
2:30 - 3:30										POCS (KAK)						
3:30 - 4:30										POCS (KAK)						

Time Table In-charge
 Prof. Kalyani Kadam

Time Table Coordinator
 Prof. Kalyani Kadam

Prof. Prabhakar Patil

Principal
 Dr. Rahul Khandagale

CAVETT'S
SIDDHANT COLLEGE OF ENGINEERING, SIDDHIVHAR PUNE-422109
 DEPARTMENT OF EAIE ENGINEERING
MASTER TIME-TABLE

Name Of Staff: Prof. Shubhangi Shelke

A-7-2021-22

SEM II

WITH EFFECT FROM:

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
8:45 - 9:45				CS (SVS)						CS (SVS)					
9:45 - 10:45				ESD (SVS)											
10:45 - 11:00	SHORT BREAK														
11:00 - 12:00	CS (SVS)			CS (SVS)											
12:00 - 03:00	ESD (SVS)				CS (SVS) PROJE					DAL	WRITE PROJE		DAL	WRITE PROJE	
1:00 - 1:40	LUNCH BREAK														
1:50 - 2:30				PBL						CS (SVS)					ESD (SVS)
2:30 - 3:10				PBL						CS (SVS)					ESD (SVS)
3:30 - 4:10				PBL						CS (SVS)					ESD (SVS)

Time Table In-charge
 Prof. Kalyani Kadam

Time table Coordinator
 Prof. Kalyani Kadam

Prof. Prashant Patil

Prashant Patil
 Principal
 Dr. Rahul Khundegate

SIDDHANT COLLEGE OF ENGINEERING, SURGURHA BELURNE

IT DEPT. *Sem-I*

ACADEMIC YEAR 2022-23

MASTER TIME TABLE

TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY	
	HE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	HE	HE	
11:00-11:30	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	
11:30-12:30	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	
12:30-1:30	LUNCH													
1:30-2:30	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	
2:30-3:30	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	
3:30-4:30	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	
4:30-5:30	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	

TIME TABLE CO-ORDINATOR

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EN-11 SE Prof. Avinash Tekale(ATT)

CAVAYETS
SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARPE, PUNE
 Department of Information Technology
 ACADEMIC YEAR 2021-22 SEM-III

MASTER TIME TABLE

DAY TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY			
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	
08-05 09-05	EM III (AT)	CNS(XYZ)	CL- OC(P)B1/ CL	WAD (AD)	CL- OC(P)B2/ CL	SE(BY)	WAD (AB)	CL- OC(P)B1/ EL	SE(BY)	WAD (AB)	CL- OC(P)B2/ EL	DBMS(X YZ)	EL- B(CBS)	DBMS(L XYZ)(S1)	EL- B(CBS)	PROJECT WORK
09-05 10-05	DBMS(X YZ)	OS- BOA(BG)	X(CBS)B2	CG(JP)	OS- BOA(BG)	X(CBS)B1	DBMS(X YZ)	OS- BOA(BG)	LIBR(K)B2	DBMS(X YZ)	EL- B(CBS)	LIBR(K)B1	DBMS(L XYZ)(S1)	LIBRARY	PROJECT WORK	
10-05 11:00				SHORT BREAK												
11:00- 12:00	PAI(RK)	OS(L)OYZ TL/ INTERNSH	SM(A)BY)	EM III (AT)	OS(L)OYZ TL/ INTERNSH	SM(A)BY)	PAI(RK)	OS(L)OYZ TL/ P-	SM(A)BY)	PAI(RK)	UP- W(AB)TY/ INTERNSH	SM(A)BY)	SE(BY)	CNS(L)OYZ TL/ INTERNSH	PROJECT WORK	
12:00- 01:00	CG(JP)	INTERNSH P-T2	INTERNE T	CG(JP)	INTERNSH P-T2	INTERNE T	CG(JP)	OC(P)B1/TA	UC(CBS)	EM III (AT)	DCS(JP)	CG(JP)	CG(JP)	PROJECT WORK		
01:00- 01:30				LUNCH BREAK												
01:30- 02:30	EM III (AT)	LIBRARY	NOT(RK)	SE(BY)	CNS(XYZ)	OC(S)JP)	LIBRARY	CNS(XYZ)	NOT(RK)	CG(JP)	LIBRARY	NOT(RK)	EM III (AT)	DS- BOA(BG)		
02:30- 03:30	DBMS(L XYZ)(S1/P	EL- B(CBS)	DCS(JP)	CG(L)P(S I/ PSD(L)RK S2	UP- Q(AB)	UC(CBS)	DBMS(L XYZ)(S2/ PBL(BG) S1	EL- B(CBS)	DCS(JP)	DBMS(L XYZ)(S1/ PBL(BG) S2	OS- BOA(L)AB)	DCS(JP)	CG(L)P(S I/ PSD(L)RK S1	DS- BOA(BG)	PROJECT WORK	
03:30- 04:30	LIBR(O)S 2	WAD (AB)	UC(CBS)	PSD(L)RK S2	LIBRARY	LIBRARY	T & P	INTERNET	INTERNET	S2	LIBRARY	UC(CBS)	PSD(L)RK S1	DS- BOA(BG)	PROJECT WORK	

Subjects Name	Class	Faculty Name
POLL, DS-BOA	TE, SE	Dr. Binodra Gupta (BG)
PALP(BD), JOT Project Work	SE, BE	Prof. Ratna Kulkarni (BK)
DBMS, DBMS, CNS, CNSL	TE, SE	Prof. H. M. S.?
EL-IT, DISTENSIONSHIP, JAC, CL-X	BE, TE	Prof. Chandrabhatra Sharma (CS)

Subject Name	Class	Faculty Name
CG, CG, DCS, CL-X	SE, BE	Prof. Jyoti Phogat (JP)
SE, SMA	SE, BE	Prof. Anand (AN)
WAD, CP-IL, DS-BOA	TE	Prof. Ashim Shinde (AS)
EM-III	SE	Prof. Anand (AN)

TT CO-ORDINATOR

HOD

PRINCIPAL

CAVNET'S
 SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE, PUNE
 Department Of Computer Engineering
 ACADEMIC YEAR 2021-22 SEM-I
 ONLINE LECTURES TIME TABLE
 Class - SE

TIME	Mon	Tue	Wed	Thurs	Fri
10:00 to 11:00 PM	DM (RP)	DM (RP)	DM (RP)	DM (RP)	DEL & D (MD)
11:00 to 12:00 PM	CG (CPS)	OOP (SY)	OOP (SY)	OOP (SY)	OOP (SY)
1:00 to 2:00 PM	FDS (KJ)	FDS (KJ)	FDS (KJ)	DEL & D (MD)	CG (CPS)
2:00 to 3:00 PM	DEL & D (MD)	DEL & D (MD)	CG (CPS)	CG (CPS)	FDS (KJ)

Subject Name	Faculty Name
Discrete Mathematics(DM)	Prof.Rupali Parpaliya (RP)
Fundamental of Data Structure(FDS)	Prof. Kavita Jadhav(KJ)
Object Oriented Programming(OOP)	Prof.Sunil Yadav(SY)
Computer Graphics(CG)	Prof.Chetana Pradip Shrivage(CPS)
Digital Electronics & Logic Design (DEL & D)	Prof Manisha Damsi(MD)

for

 Prof. Chetana Shrivage
 TT CO-ORDINATOR


 Prof. Sunil Yadav
 HOD


 Prof. U.V. Shinde
 PRINCIPAL

CAYMET'S
 SIDHANT COLLEGE OF ENGINEERING, SUDUMBARE,PUNE
 Department Of Computer Engineering
 ACADEMIC YEAR 2021-22 SEM-I
 ONLINE LECTURES TIME TABLE
 Class - TE

TIME	Mon	Tue	Wed	Thurs	Fri
10:00 to 11:00 PM	DBMS (CPS)	DBMS (CPS)	DBMS (CPS)	CN & S (AT)	CN & S (AT)
11:00 to 12:00 PM	CN & S (AT)	SPOS (KJ)	CN & S (AT)	SPOS (KJ)	IOT & ES (AB)
1:00 to 2:00 PM	SPOS (KJ)	IOT & ES (AB)	IOT & ES (AB)	IOT & ES (AB)	SPOS (KJ)
2:00 to 3:00 PM	TOC (SM)	TOC (SM)	TOC (SM)	TOC (SM)	DBMS (CPS)

Subject Name	Faculty Name
Database Management Systems(DBMS)	Prof.Chetana Shravaga (CPS)
Theory of Computation(TOC)	Prof. Seema Mahalingkar(SM)
System Programming & Operating System(SPOS)	Prof Kavita Jadhav (KJ)
Computer Network & Security(CN & S)	Prof Aparna Thakre(AT)
Elective-I Internet of Things & Embedded System (IOT & ES)	Prof.A.Bagwan(AB)

for

 Prof. Chetana Shravaga
 IT CO-ORDINATOR


 Prof. Sunil Yadav
 HOD


 Prof. Y. Shinde
 PRINCIPAL

GAYMET'S
 SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE, PUNE
 Department Of Computer Engineering
 ACADEMIC YEAR 2021-22 SEM-I
 ONLINE LECTURES TIME TABLE
 Class - BE

TIME	Mon	Tue	Wed	Thurs	Fri
10:00 to 11:00 PM	AI & R (AB)	AI & R (AB)	AI & R (AB)	AI & R (AB)	E-I DMW (SM)
11:00 to 12:00 PM	E-I DMW (SM)	E-I DMW (SM)	E-I DMW (SM)	DA (SS)	DA (SS)
1:00 to 2:00 PM	DA (SS)	DA (SS)	E-II STQA (SY)	E-II STQA (SY)	E-II STQA (SY)
2:00 to 3:00 PM	HPC (SS)	E-II STQA (SY)	HPC (SS)	HPC (SS)	HPC (SS)

Subject Name	Faculty Name
High Performance Computing(HPC)	Prof. Sushra Shinde (SS)
Artificial Intelligence & Robotics(AI & R)	Prof. A. A. Bagwan(AB)
Data Analysis(DA)	Prof. Sushra Shinde (SS)
Elective-I Data Mining & Warehousing(DMW)	Prof. Seema Mahalingkar(SM)
Elective-II Software Testing & Quality Assurance(STQA)	Prof. Sunil Yadav(SY)

for

 Prof. Chelana Shravagi
 IT CO-ORDINATOR


 Prof. Sunil Yadav
 HOD


 Prof. P.V. Shinde
 PRINCIPAL

SIDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109
 DEPARTMENT OF COMPUTER ENGINEERING
MASTER TIME TABLE Sec - A

SEM B

A.Y-2021-22

WITH EFFECT FROM 21/03/22

DAY / TIME	MONDAY				TUESDAY				WEDNESDAY				THURSDAY				FRIDAY			
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE		
8:45 - 9:45	DSA/(PK)	A/(JAC)	ELE (H/(JAB))	DSA/(PK)	OSDPA/(RPI)	M/(SY)	PRU/(MID)	A/(JAC)	M/(SY)	SC/(JAB)	OSDPA/(RPI)	OSDPA/(RPI)	CS/(JAC)	PRU/(MID)	A/(JAC)	PRU/(MID)	A/(JAC)	ELE (H/(SY))		
9:45 - 10:45	MP/(JAT)	SMA/(MID)	M/(SY)	SE/(JAB)	A/(JAC)	ELE (H/(JAB))	OSA/(PK)	SMA/(MID)	CS/(JAC)	MP/(JAT)	OSDPA/(RPI)	ELE (H/(JAB))	MP/(JAT)	OSDPA/(RPI)	M/(SY)	SE/(JAB)	OSDPA/(RPI)	M/(SY)		
10:45 - 11:00	SHORT BREAK																			
11:00 - 12:00	M-III/(MID)	OSDPA/(RPI)	CS/(JAC)	OSA/(PK)	SMA/(MID)	ELE (H/(JAB))	M-III/(MID)	WT/(SS)	CS/(JAC)	ELE (H/(JAB))	M-III/(MID)	WT/(SS)	ELE (H/(JAB))	M-III/(MID)	A/(JAC)	ELE (H/(JAB))	M-III/(MID)	SMA/(MID)	CS/(JAC)	
12:00 - 01:00	PRU/(MID)	WT/(SS)	ELE (H/(JAB))	M-III/(MID)	WT/(SS)	CS/(JAC)	MP/(JAT)	OSDPA/(RPI)	CS/(JAC)	MP/(JAT)	OSDPA/(RPI)	ELE (H/(JAB))	WT/(SS)	ELE (H/(JAB))	M-III/(MID)	WT/(SS)	OSDPA/(RPI)	ELE (H/(JAB))		
1:00 - 1:30	LUNCH BREAK																			
1:30 - 2:30	SE/(JAB)	WT/(SS)	Project Work	PRU/(MID)	WT/(SS)	Project Work	SE/(JAB)	IP	WT/(SS)	Project Work	OSA/(PK)	SMA/(MID)	INTENSHIP	Project Work	MP/(JAT)	INTENSHIP	Project Work	MP/(JAT)	INTENSHIP	
2:30 - 3:30	LH	TRP SESSION	LH	PRU/(MID)	Project Work	LH	SE/(JAB)	TRP SESSION	LH	Project Work	LH	OSA/(PK)	Project Work	LH	MP/(JAT)	Project Work	LH	MP/(JAT)	Project Work	
3:30 - 4:30	Project		Project	Project		Project	Project		Project		Project		Project		Project		Project		Project	

Time Table In-charge
 Dr. Aniket Deshpande

Time table Coordinator
 Prof. Anupam Paripallya

HOD
 Prof. Sandeep

Principal
 Dr. Ashutosh Kondegaonkar

CLASS	NAME OF CLASS COORDINATOR
SE	Prof. Anupam Thakur
TE	Prof. Anshu Chikha
BE	Prof. Suparna Shinde

CLASS	ROOM NO
SE	C-13
TE	C-24
BE	C-20

CAYMET'S
SIDDHANT COLLEGE OF ENGINEERING, SIDHUBARE PUNE-411109
 DEPARTMENT OF COMPUTER ENGINEERING
MASTER TIME-TABLE Sec - B

SEM II
 AY-2021-22
 WITH EFFECT FROM : 21/09/22

DAY / TIME	MONDAY				TUESDAY				WEDNESDAY				THURSDAY				FRIDAY	
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	
8-45 - 9-45	Code of conduct	WT/(SS)	ML/(SY)	PEU/(MO)	INTERNSHIP	ELE-IV/(SO)	LH	WT/(SS)	ELE-III/(BP)	DCA/(PK)	internship	ICSA/(AT)	SE/(AB)	OSBDA/(BP)	ICSA/(AT)	SE/(AB)	OSBDA/(BP)	
9-45 - 10-45	SE/(AB)	OSBDA/(BP)	ELE-IV/(SO)	DCA/(PK)	WT/(SS)	ELE-III/(BP)	MP/(AT)	SMAA/(SO)	ML/(SY)	PEU/(MO)	WT/(SS)	ELE-IV/(SO)	DCA/(PK)	internship	ICSA/(AT)	SE/(AB)	OSBDA/(BP)	
10-45 - 11-00																		
11-00 - 12-00	M-III	SMAA/(SO)	ICSA/(AT)	MP/(AT)	OSBDA/(BP)	ML/(SY)	M-III	OSBDA/(BP)	ICSA/(AT)	M-III	OSBDA/(BP)	ICSA/(AT)	MP/(AT)	SMAA/(SO)	ELE-III/(BP)	M-III	WT/(SS)	
12-00 - 01-00	MP/(AT)	INTERNSHIP	ELE-III/(BP)	M-III	SMAA/(SO)	ICSA/(AT)	DCA/(PK)	ICSA/(AT)	MP/(AT)	M-III	OSBDA/(BP)	ELE-IV/(SO)	M-III	OSBDA/(BP)	ML/(SY)	M-III	WT/(SS)	
1-00 - 1-30																		
1-30 - 2-30	PEU/(MO)	A/(AC)	Project Work	SE/(AB)	A/(AC)	Project Work	PEU/(MO)	A/(AC)	Project Work	SE/(AB)	A/(AC)	Project Work	PEU/(MO)	A/(AC)	Project Work	PEU/(MO)	internship	
2-30 - 3-30	DCA/(PK)	TAP SESSION	LH	LH	Class Work	LH	LH	TAP SESSION	LH	LH	Project Work	LH	LH	Project Work	LH	LH	TAP SESSION	
3-30 - 4-30	Mini Project			Mini Project														

LUNCH BREAK

SHORT BREAK

Time Table In-charge
 Dr. Aniket Deshpande

Time table Coordinator
 Prof. Binayal Pansalkar

Prof. Sandeep Yedkar

Principal
 Dr. Nikhil Khairnarayak

NAME OF CLASS COORDINATOR

SE	Prof. Ananta Thakare
TE	Prof. Archana Chitambar
BE	Prof. Sudhanshu Sahu

ROOM NO

SE	8-10
TE	8-12
BE	8-11

CAMLET'S
SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-411109
 DEPARTMENT OF COMPUTER ENGINEERING
MASTER TIME-TABLE See - B

SEM B
 A.Y.-2021-22
 WITH EFFECT FROM : 21/05/22

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY			
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	
8:45 - 9:45	Code of conduct	WT/(SS)	MU/(SV)	PPU/(MD)	INTERSHIP	ELE-N/(SD)	LH	WT/(SS)	ELE-U/(BP)	DSA/(PK)	INTERSHIP	ICS/(AT)	SE/(AB)	OSBDV/(BP)	ICS/(AT)	
9:45 - 10:45	SE/(AB)	OSBDV/(BP)	ELE-N/(SD)	DSA/(PK)	WT/(SS)	ELE-U/(BP)	MP/(AT)	SMA/(SI)	MU/(SV)	PPU/(MD)	WT/(SS)	ELE-N/(SD)	DSA/(PK)	WT/(SS)	OSBDV/(BP)	ICS/(AT)
10:45 - 11:00	SHORT BREAK															
11:00 - 12:00	M-II	SMA/(SI)	ICS/(AT)	MP/(AT)	OSBDV/(BP)	MU/(SV)	M-II	OSBDV/(BP)	ICS/(AT)	M-II	OSBDV/(BP)	WT/(SS)	ELE-N/(SD)	MP/(AT)	WT/(SS)	MU/(SV)
12:00 - 01:00	MP/(AT)	INTERSHIP	ELE-U/(BP)	M-II	SMA/(SI)	ICS/(AT)	DSA/(PK)	OSBDV/(BP)	ICS/(AT)	M-II	OSBDV/(BP)	ELE-N/(SD)	M-II	MP/(AT)	SMA/(SI)	ELE-U/(BP)
1:00 - 1:30	LUNCH BREAK															
1:30 - 2:30	PPU/(MD)	A/(AC)	Project Work	SC/(AB)	A/(AC)	Project Work	PPU/(MD)	A/(AC)	Project Work	SC/(AB)	Project Work	SC/(AB)	A/(AC)	Project Work	PPU/(MD)	INTERSHIP
2:30 - 3:30	DSA/(PK)	T&P SESSION	LH	LH	Class Work	LH	LH	Project Work	SC/(AB)	LH	LH	T&P SESSION	LH	Project Work	LH	T&P SESSION
3:30 - 4:30	Misc Project	LH	Misc Project	LH	LH	Project Work	LH	LH	Project Work	LH	LH	Project Work	LH	Project Work	LH	Project Work

Time Table In-charge
 Dr. Aniket Deshpande

Time table Coordinator
 Prof. Rupali Panpatya

Prof. Smit Yadav

Principal
 Dr. Rajni Khairnarake

CLASS COORDINATOR

SE	Prof. Aparna Thakare
TE	Prof. Archana Chavha
BE	Prof. Sushma Shinde

ROOM NO

SE	B-10
TE	B-12
BE	B-11

CVMET'S
SIDDHANT COLLEGE OF ENGINEERING, SIDDHIBARE PUNE-412109
 DEPARTMENT OF CIVIL ENGINEERING
MASTER TIME-TABLE (SEM I) - YEAR:-2021-22

DAY TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY			
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	
08:30-09:25	M-III	HWRE	E-III	EG	CM	TRF	BT&AP	CM	E-IV	BT&AP	HWRE	ACT(B1)	AC	WSE	E-IV	
09:25-10:20	EG	CM	E-IV	MOS	HWRE	E-III	EG	DSS	ACT(B2)	MOS	DSS	TRF	M-III	DSS	ACT(B2)	
10:20-10:50	R			E			C			E			S			
10:50-11:45	FM	DSS	FE	FM	DSS	E-IV	M-III	SEMINAR TI	E-III	EG	CM	E-III	SI AND BTAP		ESD (PR)	Project
11:45-12:40	MOS	EE & FM	TRF	BT&AP	WSE	MOS	MOS	WSE	TRF	AUDIT C	SEMINAR (TZ)					
12:40-01:30	R			E			C			E			S			
01:30-02:25	BT&AP	WSE	Application to Python	M-III	EE & FM	FE	M-III (TUT)	EE & FM	FE	FM	EE & FM	FE	FM	AUDIT	Applica tions in Python	
02:25-03:20	MOS (SI)	TI- DSS	B1-Python	EG(SI)	TI-CM TZ-WSS	Project	EG(S2) BT&AP- (SI)	TI-WSS TZ-CM	E-III(B1)	BT&AP- (SI)	TI-HWRE TZ-DSS	E-III(B2)	SI AND S2- MOS	TIAUT -DSS	B2- Python	
3:20-04:15	FM- (S2)	TZ- HWRE	B2-TRF	MOS (S2)											B1- TRF	

Time Table coordinator

[Signature]

HOD

[Signature]

Principal

[Signature]

SIDDHANT COLLEGE OF ENGINEERING, SUDHUMBARE PUNE-412109
DEPARTMENT OF ENGINEERING, SURVEYING
MASTER TIME-TABLE SEM - II YEAR-2021-22
SEM-II

DAY TIME	MONDAY				TUESDAY				WEDNESDAY				THURSDAY				FRIDAY			
	SE	TE	BE		SE	TE	BE		SE	TE	BE		SE	TE	BE		SE	TE	BE	
10:45-11:00	SE				SE				SE				SE				SE			
10:45-11:00	CT	RS & GIS	CM		SA	SWM (EL ID)	DHS		SUR	WWE	QSCT		SA	DR CC	DHS		PM	DRCC		
10:45-11:00	SUR	SWM (EL ID)	QSCT		CT	WWE	APC		CT	RS & GIS	CM		GTE	AC	QSCT		SA	SWM (EL ID)		
11:00-11:30	SHORT BREAK																			
11:30-12:00	LUNCH BREAK																			
12:00-12:30	GIEET (SI)	DRCC	PROJECT		SURVEY (S1)	DRCC (T1) RS & GIS	PROJECT T		PM	DRCC (T2) RS & GIS	QSCT (B1)		PBL (ASD)	WWE PR (T1)	QSCT (B2)		SUR	WWE (PR) (T2)	PROJECT T	
12:30-1:00					GTE (S2)				GTE		APC(B2)						GTE			
1:00-1:30																				
1:30-2:00	TU	SWM	APC		PM	LH	CM		LH	RS & GIS	LH		LH	LH	LH		LH	LH	LH	
2:00-2:30					CT (S2)	DRCC (T1) SWM (EL ID) (T2)	DHS (B1)		PBL (BBD)	T&P	DHS (B2)		LH	LH	LH		LH	LH	LH	
2:30-3:00	PBL (ASD)	T&P	PROJECT (STUDENT WORK TIME)		CT (S1)		CM(B2)				CM(B1)		SURVEY (S2)	DRCC (T2) SWM (EL ID) (T1)	PROJ CT (STUDENT WORK TIME)		PBL (BBD)	T&P	PROJECT (STUDENT WORK TIME)	
3:00-4:30																				

[Signature]
T.T Coordinator

[Signature]
HOD

[Signature]
Principal



CAYMET'S
SIDDHANT COLLEGE OF ENGINEERING
Sudumbare, Pune - 412109

CERTIFICATE OF COMPLETION

Subject Electronic Circuits

This is to certify that Mr/Mrs Abhijeet Arvind Nalk

Of E & TC (SE) Roll No. _____

University Exam No. _____ has satisfaction only complete the
Required number of practical/ Term Work as laid down by university.

Date:- 29/12/2021

Garguol
29/12/21

Subject Teacher

T. V. P.
Head of The E&TC Dept
Siddhant College of Engineering
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Principal
Siddhant College of Engineering
Sudumbare, Pune - 412109

CAYMET's
SIDDHANT COLLEGE OF ENGINEERING
 Sudumbare, Pune - 412109
 Department of E&TC Engineering
 A.Y. - 2021-22

Subject - Electronic Circuits

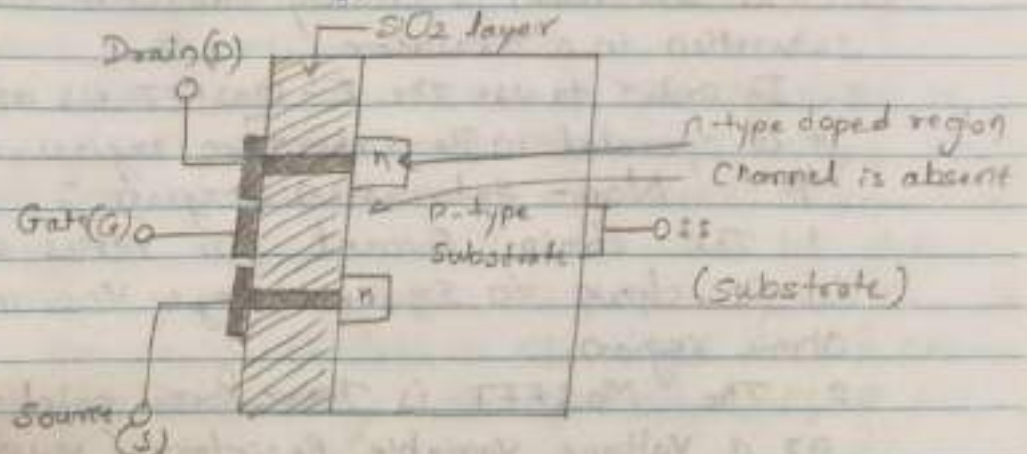
CONTENT

Sr. No.	Title of Experiment	Page No.		Sign of Teacher
		From	To	
1	Assignment 1	1	9	} <u>Gryudh</u>
2	Assignment 2	11	13	
3	Assignment 3	15	19	
4	Assignment 4	21	27	
5	Assignment 5	29	35	
6	Assignment 6	37	43	
7				
8				
9				
10				

Gryudh

Subject Teacher

- 1) Draw the constructional diagram of N channel E-MOSFET & Give drain and transfer characteristics for the same with necessary parameters.



Drain characteristics:

1. Drain characteristics is a plot of drain current I_D (on Y-axis) versus drain to source voltage V_{DS} (on X-axis) at different values of gate to source voltage V_{GS} .
2. The drain characteristics has been divided into three regions i.e. cutoff, saturation and ohmic region.

* Cutoff region:

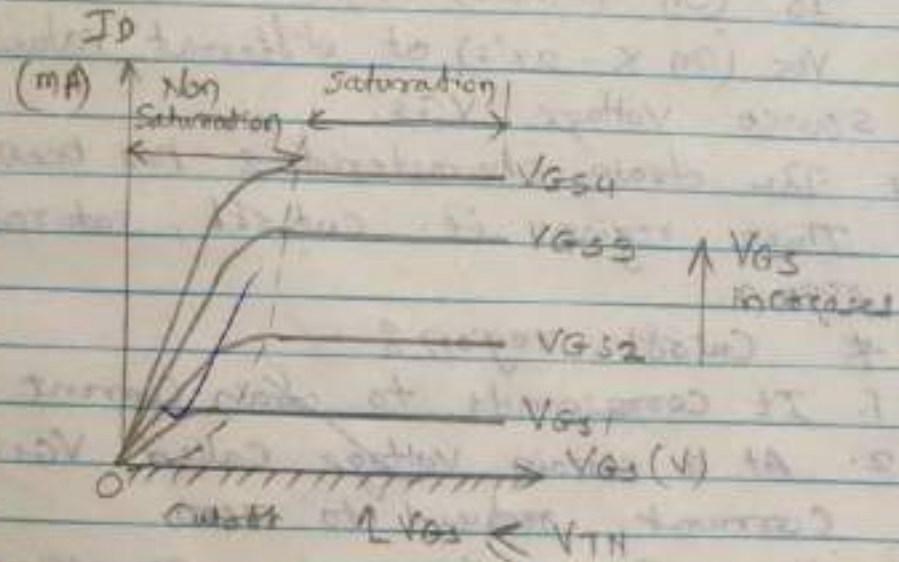
1. It corresponds to drain current $I_D = 0$
 2. At a certain voltage called $V_{GS}(off)$ the drain current reduced to zero.
 3. Hence the cutoff region corresponds to $I_D = 0$ & $V_{GS} \leq V_{TN}$
 4. The E-MOSFET operates as an open circuited switch in this region:
1. Saturation region is that portion of the characteristics

Where I_D remains fairly constant & does not change with changes in V_{DS} .

- 2. The Saturation is entirely different than the saturation in a transistor.
- 3. In order to use the E-MOSFET as an amplifier it is operated in the saturation region.

* Non-saturation region :

- 1. The drain current I_D varies with variation in the drain to source voltage V_{DS} in the Ohmic region.
- 2. The MOSFET is therefore said to be operating as a Voltage Variable Resistance (VVR) in the Ohmic region.
- 3. It is equivalent to a closed switch in this region.

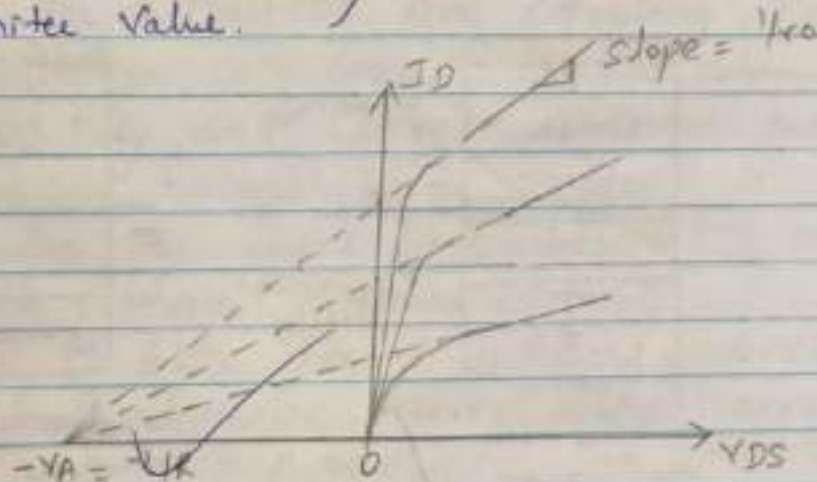


2. Explain the non ideal current voltage characteristics
- Finite r_{op} resistance
 - channel length modulation
 - Body effect
 - subthreshold conduction
 - Breakdown effect
 - Temperature effect

1. ~~Let~~ let's us assume that the MOSFET is independent of the drain to source voltage V_{DS} .

(3). The $I-V$ characteristics of MOSFET is shown in diagram. The curves can be extended by dotted lines till they intersect the x -axis at point $V_{AS} = -V_A$.

4. The r_{op} resistance (r_o) is the slope of $V-I$ curves. It should be ideally ∞ but practically it has some finite value.



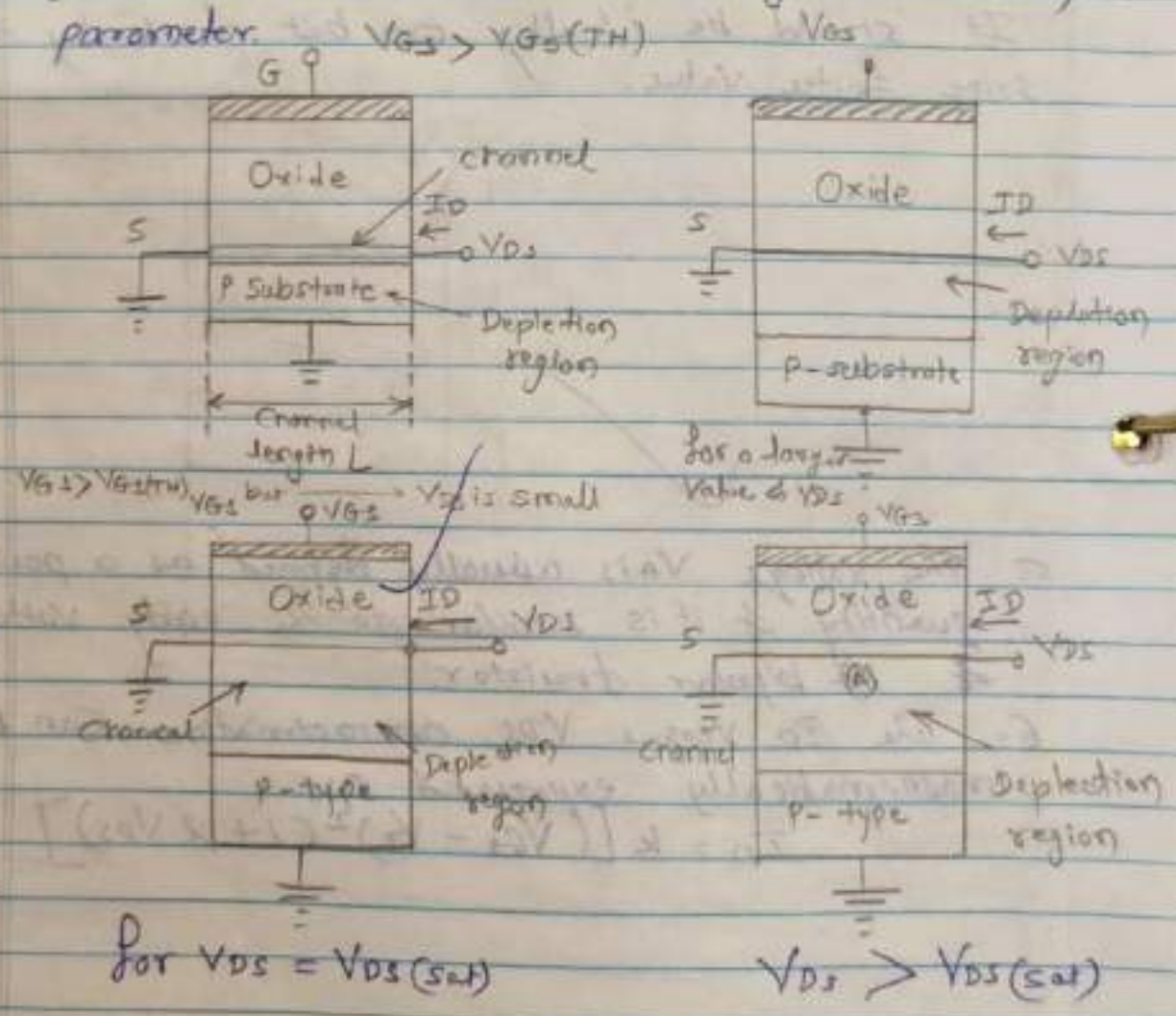
5. The voltage V_A is usually defined as a positive quantity & it is similar to the early voltage of ~~the~~ bipolar transistor.

6. The I_D versus V_{DS} characteristics can be mathematically expressed as,

$$I_D = k [(V_{GS} - V_T)^2 (1 + \lambda V_{DS})]$$

Channel length modulation

1. The finite value of I_D is due to a phenomenon called channel length modulation.
2. The voltage V_A is usually defined as a positive quantity & it is similar to the early voltage of the bipolar transistor.
3. The I_D versus V_{DS} characteristics can be expressed as $I_D = k [(V_{GS} - V_T)^2 (1 + \lambda V_{DS})]$
4. In this expression, λ is a positive quantity & called as the channel length modulation parameter.



5. For $V_{DS} > V_{DS(sat)}$, The actual point in the channel at which the inversion charge goes to zero, moves away from the drain terminal.

6. Therefore the effective channel length decreases. This phenomenon is called as channel length modulation.

iii Body effect

1. The operation of a MOSFET has been explained by assuming that the body or substrate has been connected to source.

2. When the 2 MOSFETs are conducting, the drain to source voltage will have a non zero value.

(3) When body and source are connected together, the threshold voltage V_T is constant.

4. Therefore the source terminal of M_2 will not be at the substrate potential (ground)

5. Thus M_1 & M_2 are at different potentials

6. Therefore a zero or reverse voltage appears across the source to body junction.

7. And change in the source body junction voltage will change the threshold voltage. This is called Body effect.

iv Subthreshold conduction

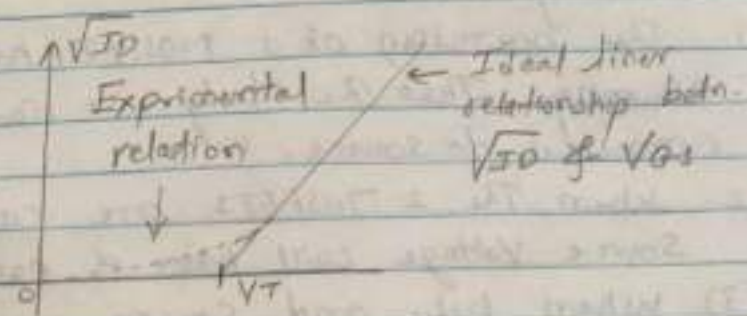
1. If an n-channel MOSFET is biased to operate in saturation region, then the ideal current voltage relationship is expressed as,

$$I_D = k (V_{GS} - V_T)^2$$

2. Taking square root of both sides we get

$$\begin{aligned} \sqrt{I_D} &= \sqrt{k} (V_{GS} - V_T) \\ &= \sqrt{k} V_{GS} - \sqrt{k} V_T \end{aligned}$$

3. This expression represents a straight line. That means $\sqrt{I_D}$ has a linear relationship with V_{GS} .



4. But practically we don't get this linear relationship. The practical characteristic is nonlinear as shown by dotted characteristics.

5. The dotted characteristics also shows that the drain current is non zero for $V_{GS} < V_T$, where theoretically it should be zero.

6. This current is called as sub threshold current.

V. Breakdown Effect.

1. Avalanche breakdown: If drain (n+) to substrate (p), p-n junction is subjected to a large reverse voltage by increasing V_{DS} . There is this junction may breakdown due to avalanche breakdown.

2. ~~Punch~~ Punch through breakdown: Another type of breakdown mechanism is punch through effect. This effect may occur if size of device becomes smaller. As the drain voltage is increased beyond a particular value, the depletion region around the drain will extend completely through the channel to source terminal. This is called as punch through.

3. Naur - avalanche or snapback breakdown:

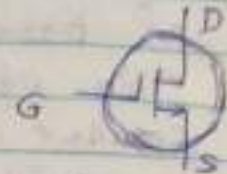
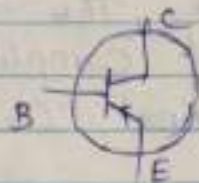
This is the third breakdown mechanism. It takes place due to second order effects within MOSFET. At the end of MOSFET devices, we may notice a ~~parast~~ Parasitic BJT acting with increase in drain voltage.

4. Breakdown due to static charge: Due to high input impedance of the MOSFET, a very small static charge accumulated on the gate can exceed breakdown. This can be avoided if we don't allow the accumulation of charge to take place on the gate capacitance.

3. Differentiate between BJT & MOSFET

Parameter	BJT	MOSFET
1. Current / Voltage Controlled device	Current	Voltage
2. unipolar / bipolar device	Bipolar	Unipolar

3. Symbol



4. Size

Small

Very small,

5. Controlling terminal

Base

Gate

6. Transfer Charac

Linear

Nonlinear

7. Thermal runaway

Can take place

Does not take place

8. Isolation of controlling terminal from device structure

Base is not Isolated

Gate is isolated

9. I/p resistance

Low/moderate

Very high.

10. Noise produced switching speed

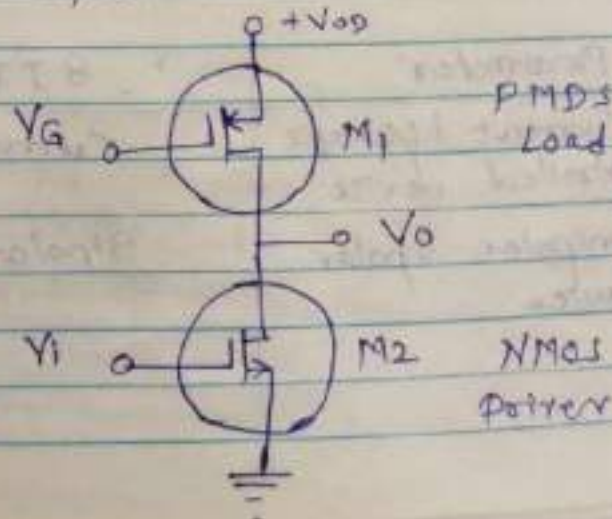
High

Very low.

Low

High.

4. Explain the principle of BiCMOS technology



1. A p-channel enhancement mode MOSFET (M_1) can be used as load for an n-channel enhancement mode MOSFET M_2 to form a Complementary MOS (CMOS) inverter.
2. The term Complementary suggests that both n-channel & p-channel MOSFET's are used in the same circuit.
3. The CMOS tech is very popular technology & it is used in both analog & digital electronic ckt's.
4. Figure shows a CMOS inverter in which the PMOS acts as a load & NMOS device acts as the driver.

Correctly

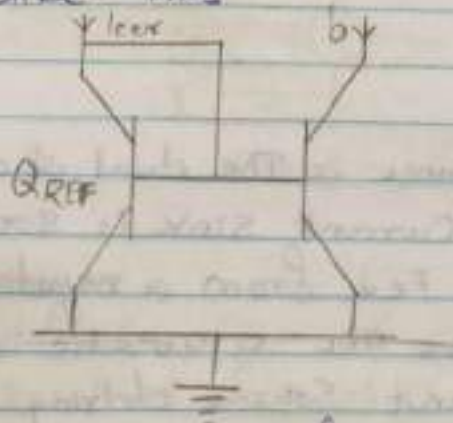
Unit - 2

11

① What is Current mirror and also state the advantages
↙ Calculate Current mirror

→ Current mirror - is explicitly used in VLSI design in order to design a constant current source which is required in some of the other parts in VLSI Circuits

This can be easily achieved by forming a circuit like - this



Here, transistor Q_{REF} is fixed biased and the collector terminal is connected to positive supply. Hence the current through that transistor remains the same.

Advantages Cascade Current Mirror

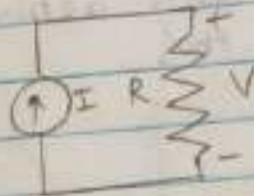
① Cascade current mirror eliminates the channel length modulation effect by keeping $V_{ds1} = V_{ds2}$ constant in the ratio:

$$I_{out} = I_{ref} \frac{(W/L)(1 + \lambda V_{ds1})}{(W/L)(1 + \lambda V_{ds2})}$$

② Improves output resistance

- ② state methods of performance improvement of current source / sink and explain any one of them.

→ Current Source is an electronic circuit that delivers or absorbs an electric current which is independent of the voltage across it.



A Current Source is the dual of a Voltage Source. The term Current Sink is sometimes used. The term Source Fed from a negative voltage supply. Figure shows the schematic symbol for an ideal current source driving a resistive load. There are two types: an independent current source (or sink) delivers a constant current, a dependent current source delivers a current which is proportional to some other voltage or current circuit.

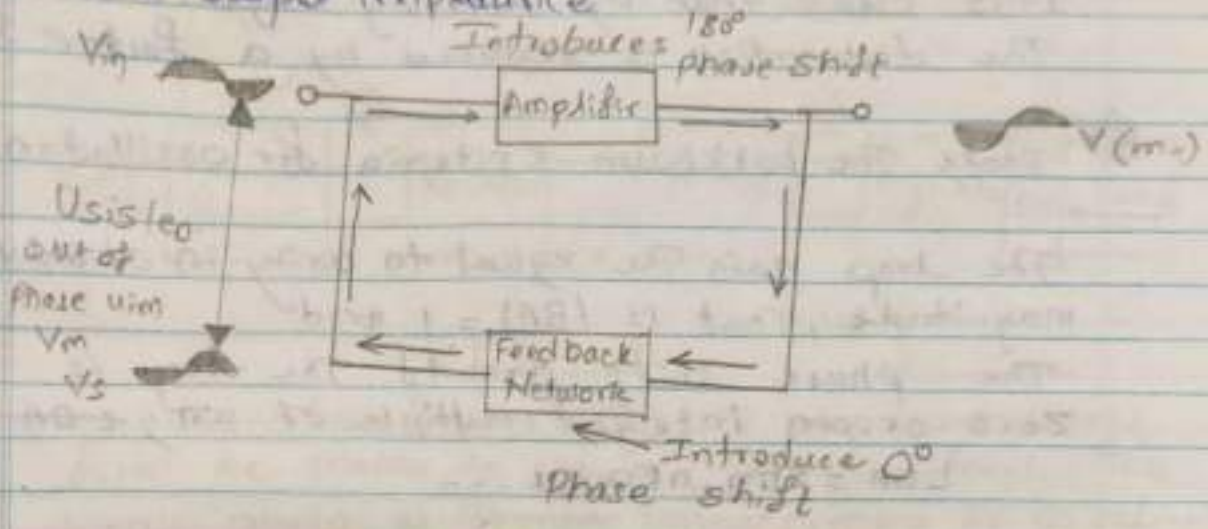
- ③ what is the effect of negative feedback on gain, stability, distortion and bandwidth

→ Negative Feedback —

In negative feedback, the feedback energy (voltage or current), is out of phase with the input signal and thus opposes it.

Negative feedback reduces gain of the amplifier, it also reduces distortion, noise and instability.

This feedback increase bandwidth and improved input and output impedance.



Gain stability -

An important advantage of negative V feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage variations.

$$A_f = A / (1 + AB)$$

Distortion -

A power amplifier will have non-linear distortion because of large signal variation. The negative feedback reduce the non-linear distortion. It can be provide mathematically that.

$$D_f = D / (1 + AB)$$

where, D = distortion in amplifier without feedback

D_f = distortion in amplifier with negative.

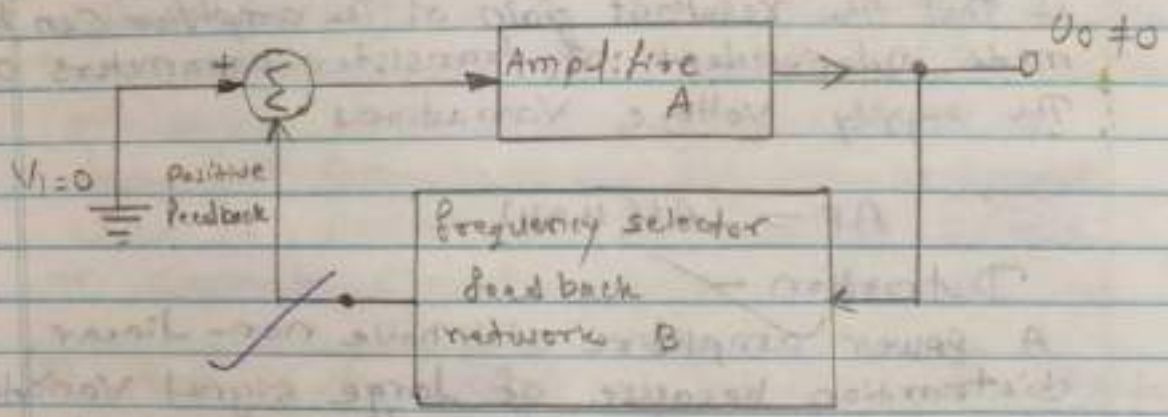
Feedback

It is clear that by applying negative feedback the distortion is reduced by a factor $(1+AB)$

④ state the Barkhausen criteria for oscillation of ckt.

→ The loop gain is equal to unity in absolute magnitude, that is $|BA| = 1$ and the phase shift around the loop is zero or any integer multiple of 2π ; $\angle BA = 2\pi n, n \in \mathbb{Z}, 1, 2, \dots$

The product BA is called as the 'loop gain'



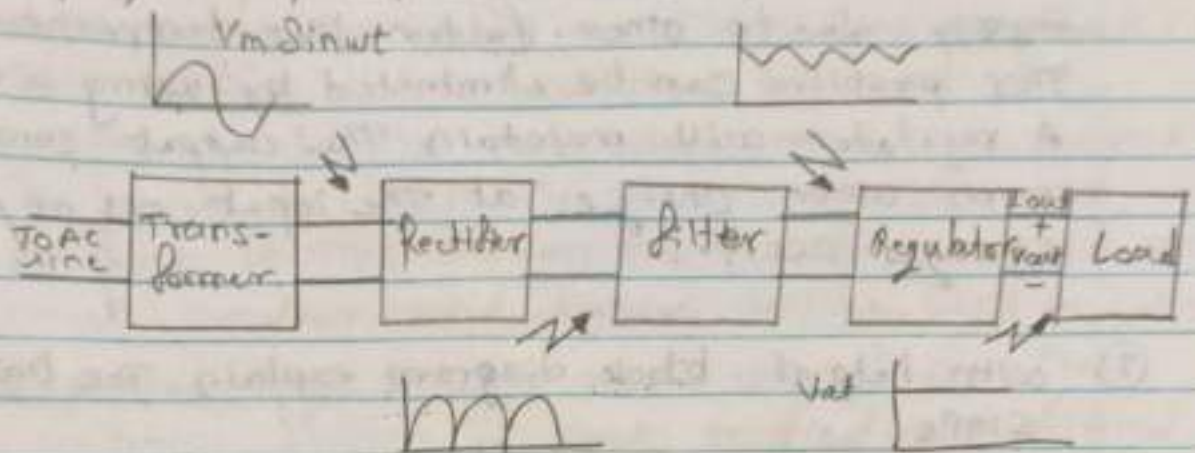
Barkhausen's Criteria of Oscillation

Angular

Unit III

15

- Q1) Draw the block diagram of regulated DC power supply. explain the function of each block in it.



1) Stepdown transformer:- It will stepdown voltage from AC mains to required voltage level. The turn's ratio of transformer is so adjusted such as required voltage value can be obtained. The O/P of transformer is given to rectifier circuit.

2) Rectifier :- is an electronics circuit consisting of diode which carries out the rectification process. The input to rectifier is an AC where its output is unidirectional pulsating DC. Usually a full wave rectifier bridge rectifier is used to rectify both half cycle of the AC supply.

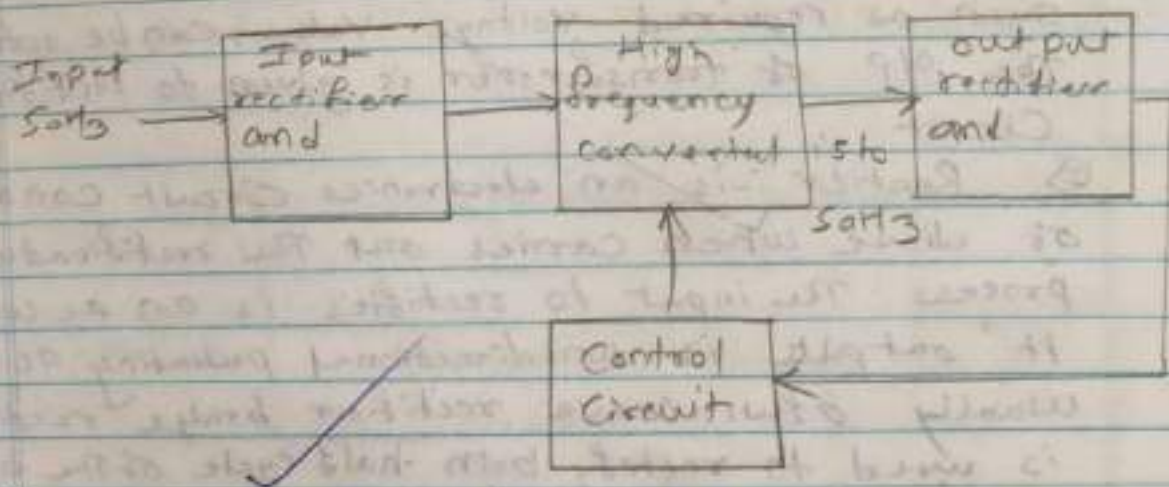
3) Filter :- The rectified voltage from rectifier is a pulsating DC voltage having very high ripple content hence filter is used.

4) Regulator :- This is the last block in regulated DC power supply. The output voltage as current will change as load varies when there is change in AC input from AC mains as due change in

Load current at the output of the regulated power supply due to other factor like temperature change. This problem can be eliminated by using a regulator. A regulator will maintain the output constant even when change at the input or any other changes occur.

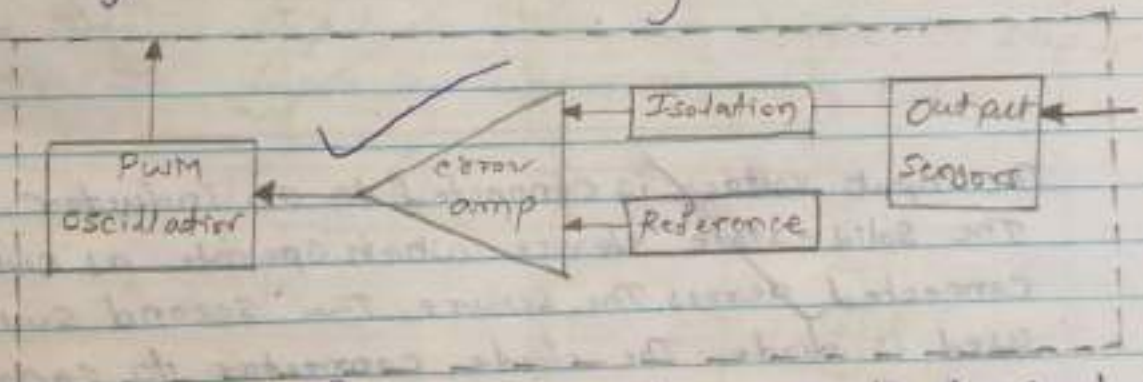
② with help of block diagram explain the basic SMPS.

→ The working of SMPS can be understood by following figure.



① Input stage:- The AC input signal 50Hz is given directly to rectifier and filter circuit combination without using Autotransformer. This output have many variation and the capacitance value of one capacitor should be higher to handle one up fluctuation. This unregulated DC is given to central switching section of SMPS.

- 2) Switching Section :- A fast switching devices such as power transistor or MOSFET is employed in this section which switched on and off according to the variations and this output is given to primary of the transformer present in this section. The transformer used are much smaller and lighter, unlike used in COTs.
- 3) output stage :- The output signal from the switching section is again rectified and filtered to get the required DC voltage which is given to the control circuit which feedback circuit. The final output is obtained after considering the feedback signal.
- 4) control unit :- This is feedback circuit has many section. The following figure shown below.

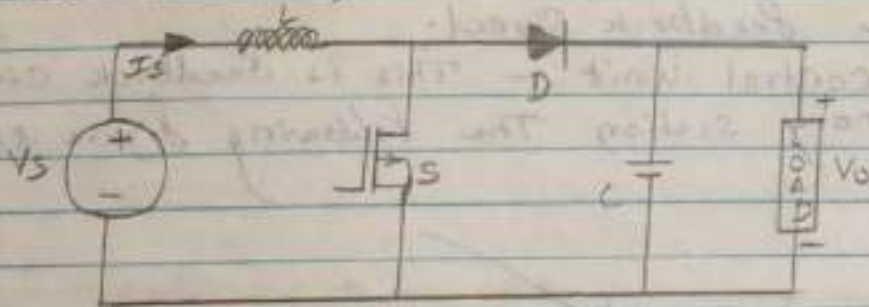


The above figure explain inner part of a control unit. The output sensor the signal and joins it to the control unit. The signal is isolated from the other section so that sudden spikes should not affect the circuitary. A reference voltage is given as one input along with signal to error amplifier which is comparator that compares

This signal with required signal level. by controlling the chopping frequency the final voltage level is maintained. This is controlled by comparing input given to error amplifier, whose output help to decide whether to increase as oscillator produces a standard PWM wave fixed frequency.

3) Describe the boost converter or buck boost converter.

→ Boost converter:- DC-DC converter are also known as chopper. A step up chopper is called as boost converter. It increase the input DC voltage to specified DC output voltage. A typical boost converter is shown below.



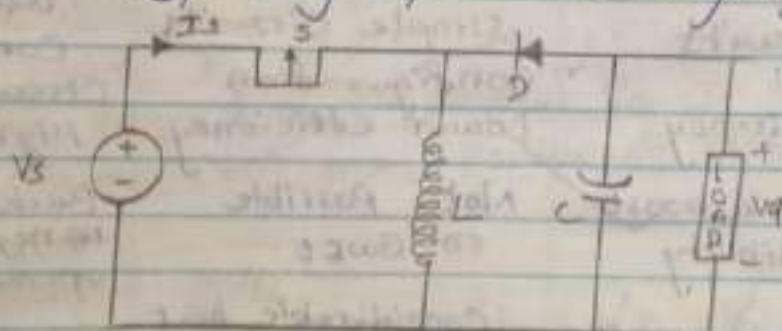
The input voltage is connected to an inductor.

The solid-state device which operate as switch is connected across the source. The second switch used is diode. The diode connects to capacitor and the load and two are connected in parallel.

The inductor connected to input source load consist constant current and thus the boost converter is seen as constant current input source. The controlled switch is turned on/off by using PWM. PWM can be time based or frequency based. Boost converter has two mode of operation.

1st mode switch is operated and current through inductor is made continuous. In this energy is stored. 2nd mode switch is off and diode is on. In this mode, energy stored in inductor is released. This helps to maintain flow of current in same direction.

2) Buck boost Converter: The buck boost converter is type of DC-DC converter (also known as chopper) that has an output voltage magnitude either greater than or less than the input voltage. magnitude it is equivalent to flyback converter using a single inductor instead of transformer. two different topologies are called as buck boost converter. DC-DC converter also known as chopper. Here we have a look at buck boost converter which operates as DC-DC step down converter as DC-DC step up converter depending upon the duty cycle.



The input voltage is connected to solid state device. The second switch used is a diode. The diode is connected in reverse direction of power flow from source to a capacitor, and load are connected in parallel. The controlled switch is to on and off using PWM. PWM can be time base as frequency.

1st mode. switch is on and Diode off. Current flow to Inductor and back to dc input source. Inductor store charge during this when switch is off polarity Inductor reverse and current through load through diode and back to Inductor.
2nd Mode. switch off and diode ON.

4) comparison between linear and switching mode regulator.

	Linear Regulator	Switching Regulator.
1) Components used	Linear components such as resistor Load to regulator	Switch regulator switch elements to transform the incoming supply in pulsed voltage. MOSFETS are used.
2) Circuits	Simple circuits configuration	Complex circuit used
3) efficiency	Lower efficiency	High efficiency.
4) Buck boost possibility	Not possible to Boost	Buck / boost / or negative voltage operation positive
5) Heat generation	considerable heat generation	Low heat generation
6) Noise levels	Low noise	Increase noise.

through

ASSIGNMENT NO-4

Q.1. Analyze the dual input balanced output differential amplifier to obtain the following:

- 1) Differential gain 2) common mode gain
- 3) O/P resistance 4) I/P resistance.

Ans: To perform the ac analysis of dual input balanced output differential amplifier, following are the steps -
 Step 1 - Set the dc voltages $+V_{CC}$ & $-V_{EE}$ to zero i.e. short them to ground

Step 2 - Replace the transistors Q_1 & Q_2 with their small signal T-equivalent models.

ii) Fig (a) shows the resulting ac equivalent circuit of the dual - input balanced - output differential amplifier.

iii) As $I_{E1} = I_{E2}$, we can write that $r_{e1} = r_{e2}$. Hence the ac emitter resistance of transistor Q_1 & Q_2 are equal to r_e i.e. $r_{e1} = r_{e2} = r_e$

iv) The voltage across each collector resistor R_c is out of phase by 180° with V_{s1} & V_{s2} . Note that polarity assigned to O/P voltage V_o . It indicates voltage at collector (2) is more positive to voltage at c₁.

i) Differential gain -
 Output Voltage $V_o = \frac{R_c}{r_e} (V_{s1} - V_{s2})$

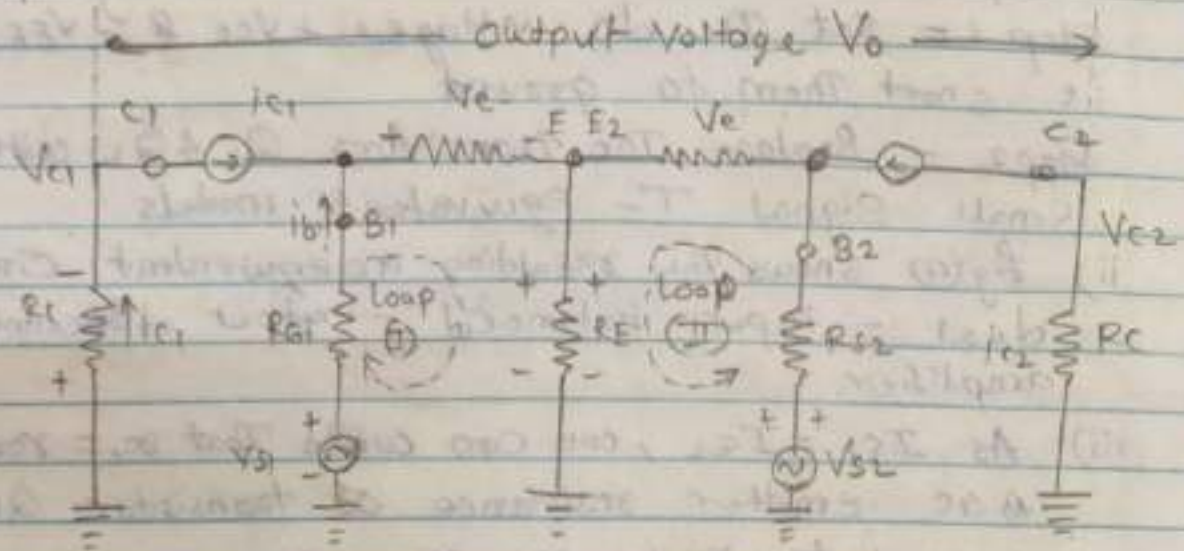
In this equation the term $V_{s1} - V_{s2} =$ differential i/p voltage V_d .

$$V_{s1} - V_{s2} = V_d$$

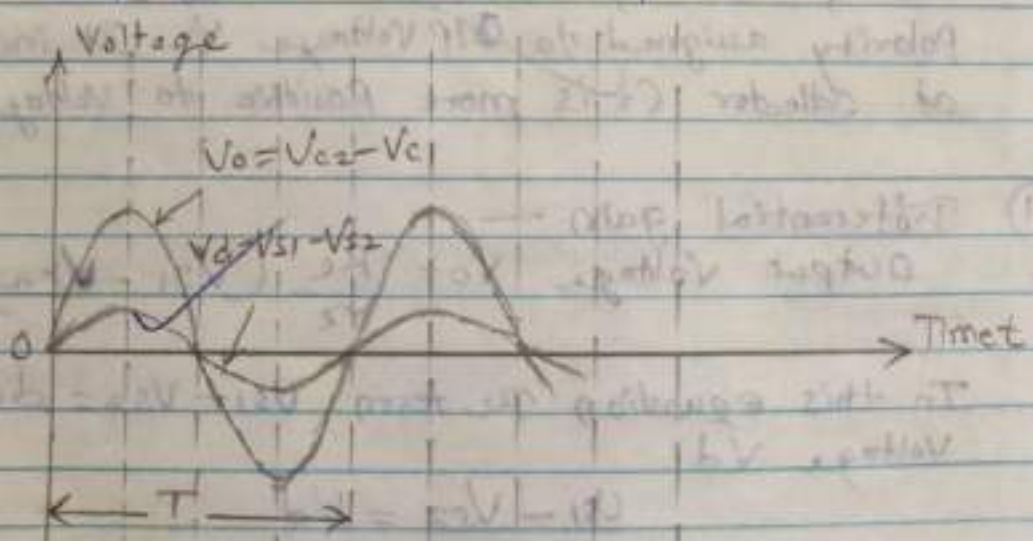
The voltage gain of dual input balanced output differential amplifier

$$A_d = \frac{V_o}{V_d} = \frac{R_c}{r_e}$$

A positive gain indicates that V_o & V_d are in phase with each other.



(a) AC equivalent circuit of dual input balanced output differential amplifier



(b) Input and output waveforms.

This expression shows that voltage gain does not depend on R_E .

Differential amplifier only the differential voltage ($V_{s1} - V_{s2}$) The i/p & o/p voltage waveforms are shown in fig (b)

(2) Input Resistance (R_i) -

i) It is defined as a equivalent resistance measured at any of i/p terminals with the other terminal connected to ground

(ii) Value of R_{i1} -

The differential i/p resistance seen from V_{s1} is given

$$\text{by } R_{i1} = \left. \frac{V_{s1}}{i_{b1}} \right|_{V_{s2}=0}$$

but $i_{b1} = i_{e1} / \beta_{ac}$

$$\therefore R_{i1} = \left. \frac{V_{s1}}{i_{e1} / \beta_{ac}} \right|_{V_{s2}=0} = 0$$

Substituting the value of i_{e1} & $V_{s2} = 0$ we get

$$R_{i1} = \beta_{ac} \left[2r_e + R_E \right] = 2\beta_{ac} r_e + \beta_{ac} R_E$$

This is the expression for R_{i1}

iii) Value of R_{i2} -

The differential i/p resistance seen from V_{s2} is given by

$$R_{i2} = \left. \frac{V_{s2}}{i_{b2}} \right|_{V_{s1}=0} = 0$$

but $i_{b2} = i_{e2} / \beta_{ac}$

$$\therefore R_{i2} = \left. \frac{V_{s2}}{i_{e2} / \beta_{ac}} \right|_{V_{s1}=0} = 0$$

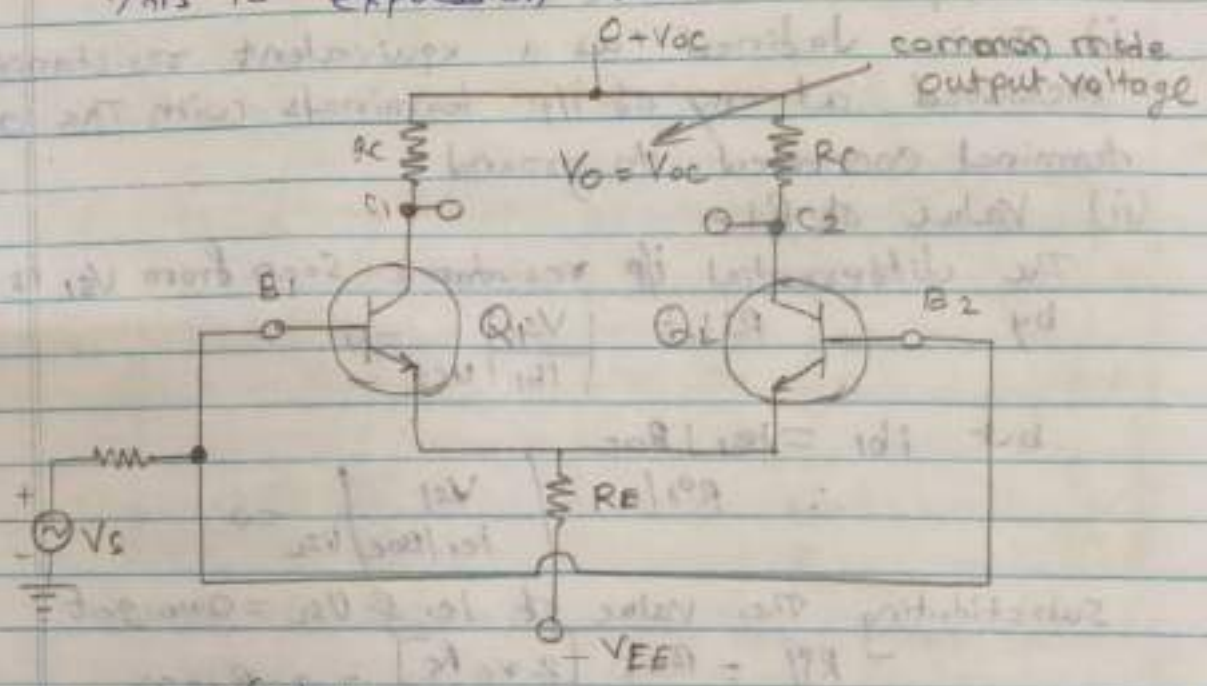
Substituting the value of i_{e2} if $V_{s1} = 0$ we get

$$R_{i2} = \frac{\beta_{ac} r_e (r_e + 2R_E)}{(r_e + R_E)}$$

Assuming $R_E \gg r_e$ we get

$$\therefore R_{i2} \approx 2 \beta_{ac} r_e$$

This is expression for R_{i2} .



(C) Arrangement to measure the common mode gain A_{cm}

(3) Output Resistance (R_o)

- i) o/p resistance R_o is defined as equivalent resistance measured at any of o/p terminals w.r.t. ground
- ii) That means R_{o1} is measured betⁿ collector C1 to ground & R_{o2} is measured betⁿ collector C2 to ground.
- iii) from Fig (a) we conclude R_{o1} & R_{o2} have same value equal to R_C .

$$\therefore R_o = R_{o1} = R_{o2} = R_C$$

4) Common mode gain -

- i) The common mode voltage gain can be obtained by applying a common signal i/p V_s to both i/p as shown in Fig (c) & measuring the common mode o/p voltage V_{oc} betⁿ the collector of two transistor
- ii) The common mode voltage gain is given by

$$A_c = \frac{V_{oc}}{V_s}$$

Q.2 Define the characteristics of a practical op-amp

- 1) I/P offset voltage
- 2) CMRR
- 3) PSRR
- 4) slew rate

Ans: 1) I/P offset voltage -

- i) A small differential i/p voltage that is required to be applied to an op-amp in order to make its o/p zero is called as i/p offset voltage.
- ii) The i/p offset voltage is denoted by V_{ios} . The i/p offset voltage is normally in a few mV range. The value of i/p offset voltage is temp. dependent. Ideally V_{ios} should be equal to zero.

2) Common Mode Rejection Ratio (CMRR) -

- i) For an op-amp, the common mode rejection ratio is defined as the ratio of differential gain to common mode gain.

$$\therefore \text{CMRR (P)} = \frac{A_d}{A_{cm}}$$

- ii) CMRR indicates the capability of the op-amp to successfully reject the common mode signals. CMRR is denoted by Pf it is generally expressed in decibels (dB)

iii) CMRR should be as high as possible to reject the common mode signals such as noise successfully

3) Power Supply Rejection Ratio (PSRR) -

i) The change in an op-Amps I/P offset voltage (V_{ios}) due to variation in the supply voltage is called as power supply rejection ratio $R(PSRR)$

ii) Mathematically $PSRR = \frac{\Delta V_{ios}}{\Delta V}$

Where ΔV_{ios} = change in i/p offset voltage

ΔV = Change in the supply voltage

It expressed in micro Volts per Volt or in decibels

(iii) The value of PSRR should ideally be equal to zero & practically it should be small as possible.

4) Slew Rate -

i) Slew rate defined as max^m rate of change of op voltage per unit time Mathematically

$$SR = \frac{dV_o}{dt} / \text{max}^m \text{ Volts}/\mu\text{s}$$

(ii) The unit of slew are Volts / microseconds.

Q3 Why DC level shifting is required in LTC?
Draw & explain various level shifting circuits

⊕ When the I/P signal passes from one stage to the other its DC level goes on increasing

Due to increased DC level output voltage gets distorted. It also limits the max^m output

Voltage swing

③ There fore we have to use a level shifting stage to bring the dc level to zero volts circuit ground

4) There are number of level shifter or translator circuits available

2) DC level shift stage using PNP-NPN transistor -

i) Fig (e) shows the dc level shifter circuit using PNP-NPN transistor

ii) Voltage across R_1 i.e. $V_{R1} = V_{CC} - V_{BE1} - V_{in}$

$$\text{There fore current } I_1 = \frac{V_{R1}}{R_1} = \frac{(V_{CC} - V_{BE1} - V_{in})}{R_1}$$

$$\text{O/P Voltage } V_{out} = I_1 \times R_2$$

$$V_{out} = R_2 \frac{(V_{CC} - V_{BE1} - V_{in})}{R_1}$$

iii) #

iii) By adjusting the value of R_2 it is possible to adjust the dc shift at o/p to desired value

3) level shifter using a constant current source -

i) Fig (f) shows the constant current source or current mirror.

ii) The constant current source or current mirror circuit can adjust the value of I_c in such away that get zero dc voltage at the output

Q4. What is slew rate & what are its causes?
Derive an expression for max. freq. of operation for desired op swing in terms of slew rate.

Ans - Definition - slew rate defined as the maximum rate of change of o/p voltage per unit time. Mathematically it is expressed.

$$SR = \frac{dV_o}{dt} / \text{max}^m \text{ Volts}/\mu\text{s}$$

- ii) The unit of slew rate are Volts/microseconds
- iii) Slew rate decides the capability of op-amp to change its o/p rapidly hence it decides the highest frequency of operation of a given op-amp
- iv) The value of slew rate depends on the change in voltage gain therefore it is generally specified at unity gain.
- v) Slew rate should be ideally & practically as high as possible.
- vi) Value of slew rate of an op-amp decides the max^m frequency (f_o) which can be amplified by the op-amp without introducing any distortion

$$f_m = \frac{S}{2\pi V_m}$$

where V_m = Peak i/p Voltage.

Frequency

unit 5

Q1. Explain with the help of circuit Diagram the operation of an OP-Amp inverting & non-inverting amplifier. Derive an expression for the voltage gain of this amplifier.

Ans:- The Inverting Amplifier -

- i) The circuit Diagram of an inverting amplifier is as shown in fig (a)
- ii) The signal which is to be amplified is applied at the inverting (-) input terminal of OP-Amp
- iii) The signal to be amplified (V_s) has been connected to inverting terminal via resistance R_1
- iv) The other resistance R_F connected betⁿ the op & inverting i/p terminals called as feedback resistance.
- v) The non-inverting (+) input terminal is connected to ground.
- vi) As the - inverting OP-Amp is an ideal one. its open loop voltage gain $A_V = -\infty$ & i/p resistance $R_i = \infty$
- vii) The op wave forms are shown in fig (b)
- viii) From fig (a) $V_o = |A_V| \times V_d$

$$\therefore V_d = \frac{V_o}{(A_V)}$$

where A_V = open loop gain of OP-AMP

As we know A_V , of open loop is ∞

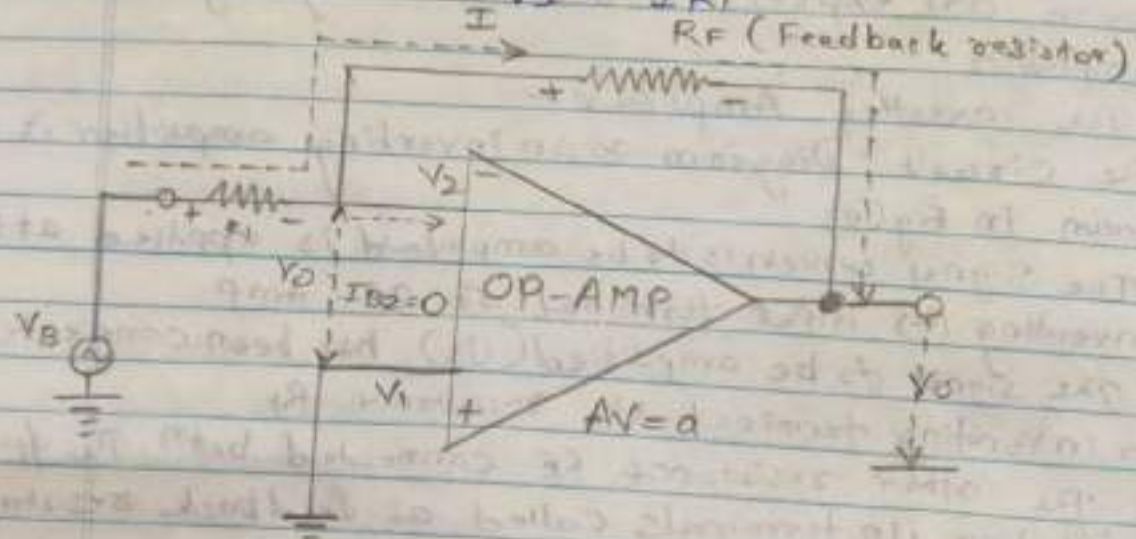
$$\therefore V_d = \frac{V_o}{\infty}$$

$$\text{But } V_d = 0 \text{ But } V_d = V_1 - V_2$$

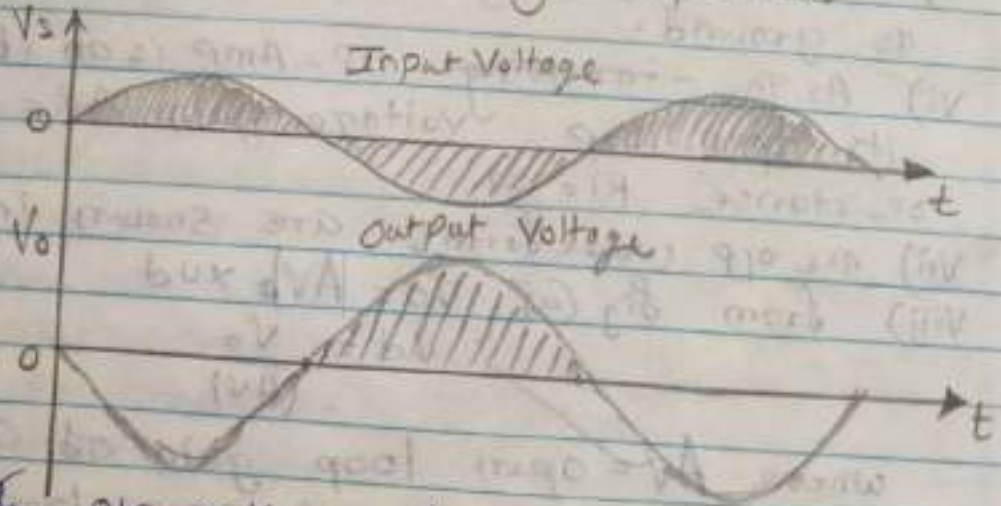
$$\therefore V_1 - V_2 = 0$$

Substituting $V_1 = 0$ we get $V_2 = 0$

Thus V_2 is at ground potential
 $R_1 = \infty$ The i/p voltage is given by
 $V_s = I R_1$



(a) Inverting amplifier.



\checkmark o/p voltage $V_o = -I R_F$
 closed loop gain $A_{VF} = \frac{V_o}{V_s}$
 Substituting V_o of V_s $A_{VF} = \frac{-I R_F}{I R_1}$
 $= \frac{-R_F}{R_1}$
 $\therefore V_o = A_{VF} \times V_s$

2) Non-inverting amplifier -

i) The non-inverting amplifier using op-amp shows in fig (c)

ii) Here the signal which is to be amplified is applied to the non-inverting (+) input terminal of op-amp & the inverting (-) i/p terminal is connected to ground via R_1

iii) The negative feedback is introduced in this circuit via feedback resistance R_F which is connected b/w of inverting (-) i/p terminal of op-amp.

iv) As we are using an ideal op-amp $R_i = \infty$. Therefore

$$I_1 = I_2 = 0$$

v) Therefore voltage across R_1 by

$$V_2 = \frac{R_1}{(R_F + R_1)} V_o$$

$$V_1 = V_2 = V_2$$

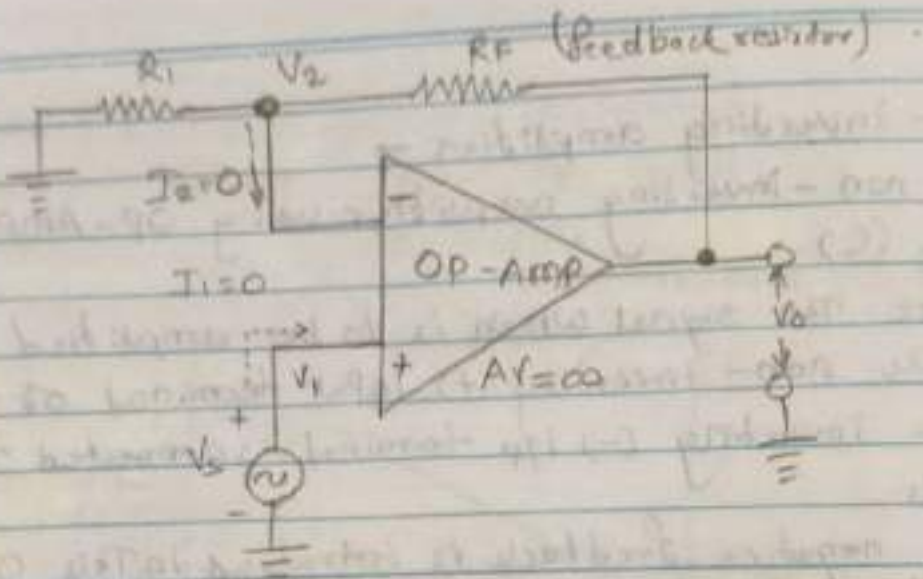
vi) Substituting expression for V_2 ,

$$\therefore V_1 = \frac{R_1}{(R_F + R_1)} V_o$$

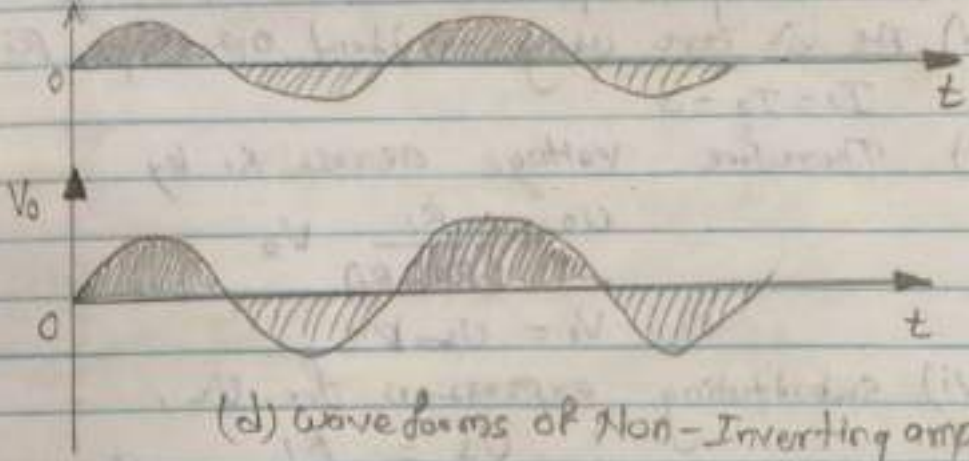
$$\checkmark \text{ A.V.F.} = \frac{V_o}{V_1}$$

$$= \frac{R_1 + R_F}{R_1} = 1 + \frac{R_F}{R_1}$$

$$\therefore V_o = \text{A.V.F.} \times V_1$$



(c) Non-inverting amplifier
Input Voltage V_s



(d) waveforms of Non-Inverting amplifier

Q2. Explain the operation of device. The expression for output voltage of differential input differential output amplifier.

Ans: (i) Differential input voltage is the maximum voltage that can be supplied to the input of pins without causing damage. The voltage is suitable as a reference for the inverting and non-inverting terminals.

(ii) A differential output voltage is the difference between the values of two AC voltages 180° out of phase present at the o/p terminal of an amplifier.

when we apply differential i/p voltage to the i/p terminal of an amplifier.

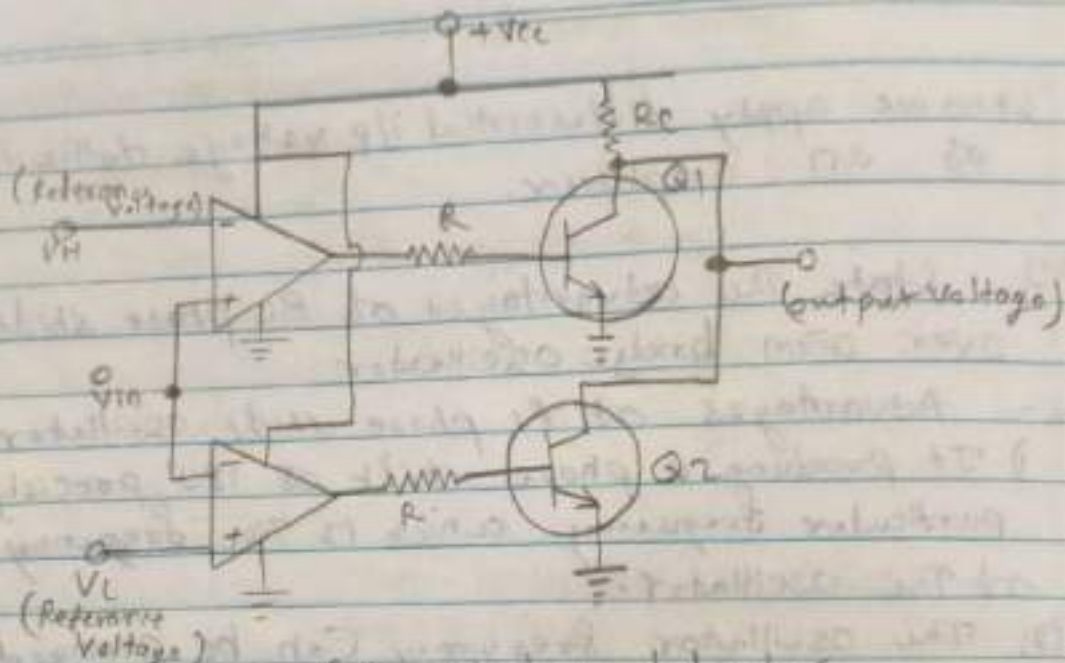
Q3. State the advantages of RC phase shift oscillator over Wien bridge oscillator

Ans:- Advantages of RC phase shift oscillator -

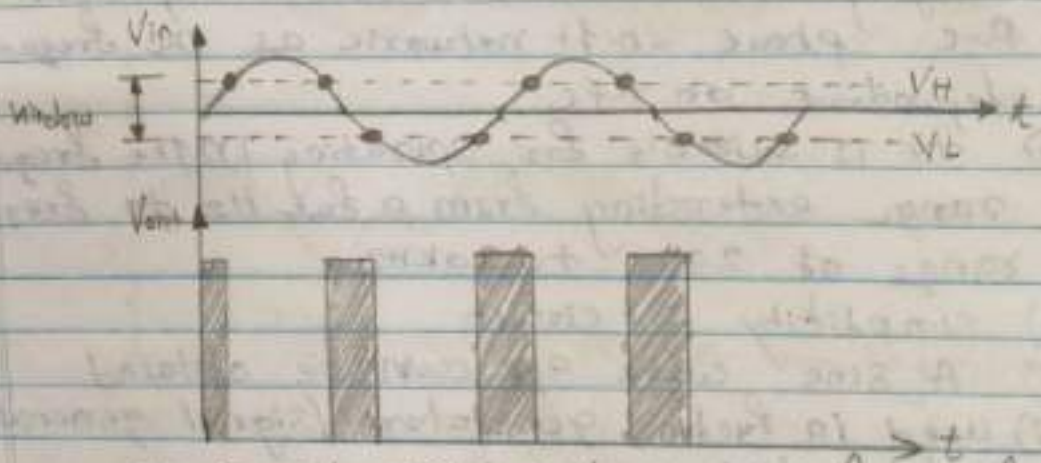
- 1) It produces a phase shift of 180° precisely only at the particular frequency which is the frequency of operation of the oscillator.
- 2) The oscillator frequency can be changed by changing either the resistors or capacitor in the R-C phase shift network as the frequency is dependent on R/C.
- 3) It is suitable for operating in the frequency range extending from a few Hz to frequency range of 20Hz to 20kHz.
- 4) Simplicity of circuit.
- 5) A sine wave o/p can be obtained.
- 6) Used in function generators (signal generator used in laboratories).
- 7) It doesn't require any negative feedback & stabilization arrangements.

Q.4. Brief application of comparator & explain any one of them.

Ans:- Application of comparators -



(e) window detector



Input and output voltage waveforms for a window detector

- 1) In signal generation & transmission
- 2) Automatic control of measurements
- 3) A/D Converter
- 4) level detector of window comparator
- 5) V-F Converter
- 6) switching regulator.

Window Comparator -

- i) The window detector circuit using two comparators is shown in Fig (e).
- ii) The window detector circuit is used for detecting whether an unknown voltage V_{in} falls within a specified voltage band called window.
- iii) V_H & V_L are two reference voltage with $V_H > V_L$ & V_{in} is the input voltage.
- iv) If V_{in} is betn two reference voltage i.e. $V_L < V_{in} < V_H$ Then the op of both comparators will be low.
- v) Collector voltage i.e. o/p voltage will be equal to V_{CC} .
 $\therefore V_o = +V_{CC} : \text{For } V_L < V_{in} < V_H$.
- vi) This will turn off transistor Q_1 but saturated transistor Q_2 & the o/p voltage will be V_{CC} i.e. low.
 $\therefore V_o = V_{CC} = \text{low} : \text{For } V_{in} < V_L$
- vii) If $V_{in} > V_H$, Then o/p of comparator 1 will be high & that of comparator 2 will be low.
- viii) Transistor Q_1 will saturate & Q_2 will remain off & the o/p voltage will be V_{CC} i.e. low.
 $\therefore V_o = V_{CC} = \text{low} : \text{For } V_{in} > V_H$
- ix) Conclusion - A High voltage indicator that the i/p voltage is within the window whereas a low o/p voltage indicator that i/p voltage is out window.
- x) The i/p voltage waveform for a window detector are as shown in Fig (f).

Conclude:

Unit 6

37

Q.1 Explain The basic principle of D to A converter.

- Ans: (i) The block diagram of DAC shown in fig (a)
- (ii) The basic building blocks of DAC are - A resistive network, digitally controlled electronic switches and a voltage reference of C to V converter.
- (iii) A digital I/P code is applied to resistive network via the digitally controlled switches.
- (iv) The digitally controlled switches are turned on or off by digital I/P bits.
- (v) The o/p current can be converted into proportional voltage with help of C to V converter.
- (vi) Thus we obtain analog o/p voltage proportional to digital I/P code.
- (vii) The actual digital to analog conversion takes place within the resistive network.

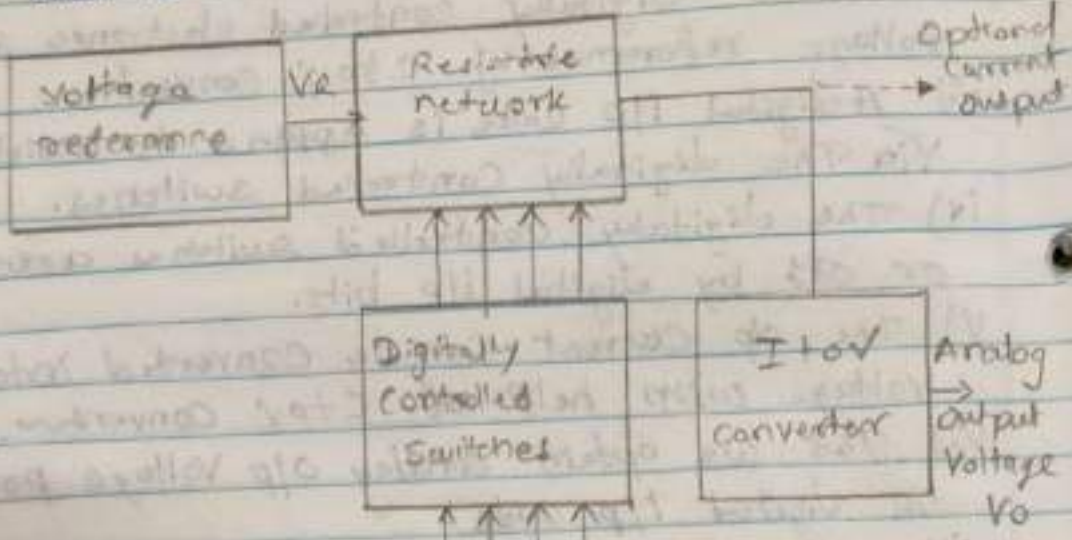
Q.2 Explain the following types of errors 1) linearity error 2) offset error 3) Gain error.

Ans:- Linearity Error-

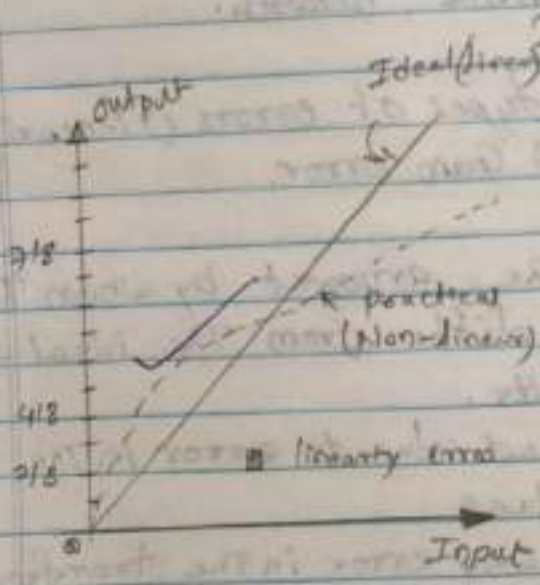
- i) This is defined as the amount by which the actual o/p of a DAC differs from the ideal straight line transfer characteristics.
- ii) This error is introduced due to error in the current source resistance value.
- iii) Fig (b) shows the linearity error in the transfer characteristics of DAC.

2) Offset Error -

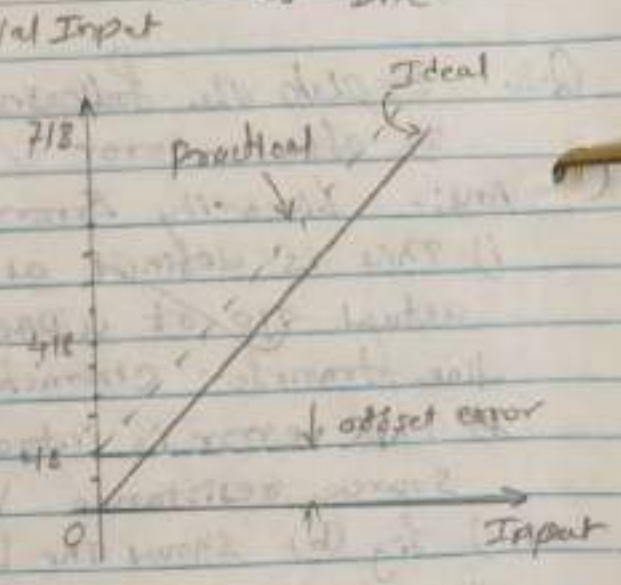
i) Ideally when all the digital i/p are 0, the analog o/p also is.



(a) Block diagram of DAC



(b) Linearity error in transfer characteristic of D/A Converter



(c) Offset error in transfer characteristic of D/A Converter

expected to be 0

- ii) As shown in Fig (c) same non-zero analog o/p voltage is present even for a zero digital i/p.
- iii) This called offset error. The offset error is due to the offset voltage of op-amp & leakage currents in the switches.

3) Gain Error -

i) In DAC we use a current to voltage converter. Therefore the analog o/p of DAC is dependent on the gain of this converter.

ii) The gain error is defined as the difference betⁿ the theoretically calculated gain & practically obtained gain of I-to-V converter.

iii) This error is produced due to error in feedback resistor value. The gain error is as shown in Fig (d)

Q3 What is PLL? Describe transfer characteristics of PLL. mention any four application of PLL in radio communication.

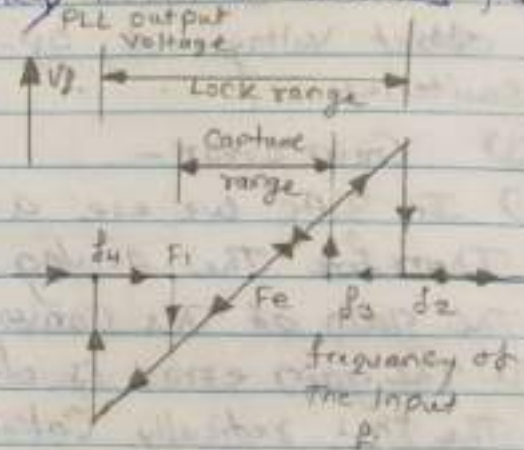
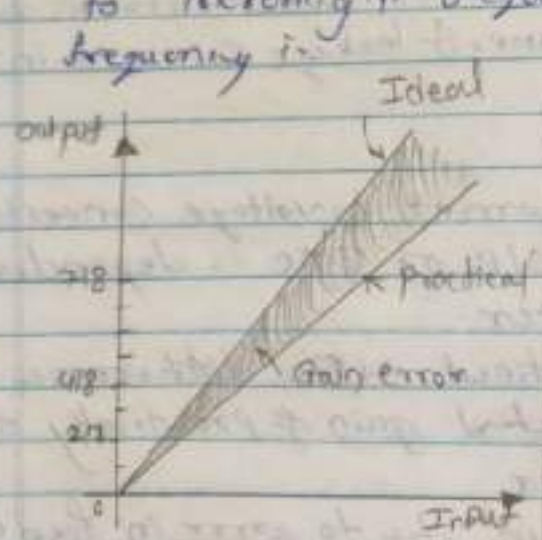
Ans - Definition - A phase lock loop (PLL) is a control system that generates an output signal whose phase is related to phase of an i/p signal. The phase locked loop (PLL) is a closed loop system. Its application is to lock its output frequency and phase to the frequency & phase of i/p signal.

PLL Transfer Characteristics -

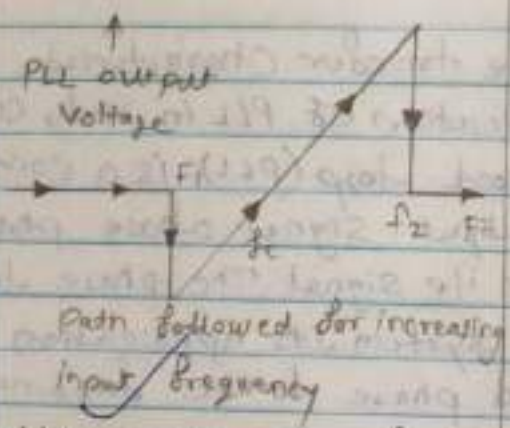
- i) Fig (c) shows the transfer characteristics of a PLL.
- ii) It is a graph of PLL o/p voltage V_f versus the frequency of input signal i.e. f_i .
- iii) Transfer characteristic indicates that the PLL exhibit property of hysteresis like B-H curve.

Operation with increasing input frequency —

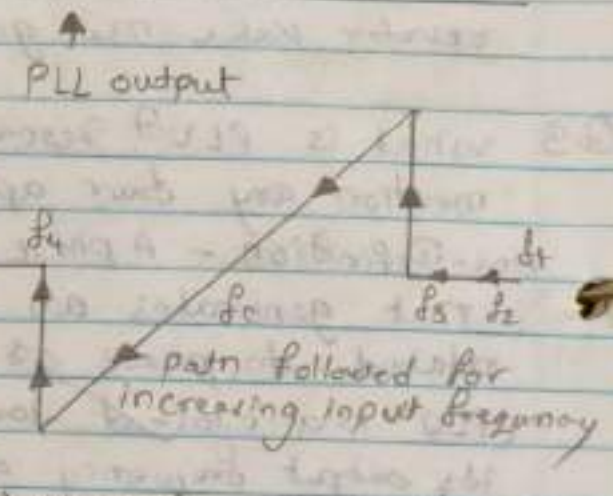
iv) Fig (d) shows that the PLL does not respond to increasing its frequency F till it reaches the frequency F_c .



(e) transfer characteristics of a PLL



(f) transfer curve for the increasing input frequency



(g) Transfer curve for the decreasing input frequency

- v) This frequency is called as the lower edge of capture range.
- vi) For increasing i/p frequency above f_1 , the PLL gets locked to the input frequency.
- vii) When $f_1 > f_2$ i.e. the upper edge of the lock range, the PLL loses lock, output voltage V_o reduce to 0 & VCO frequency will return to f_c .
- viii) Thus the path followed for increasing input frequency is from f_1 to f_2 & then f_c as shown in fig (b)
- Operation with decreasing input frequency -
- i) The path followed by the output voltage with the i/p frequency decreasing will not be the same as that followed when the i/p frequency was increasing.
 - ii) This is shown in fig (c)
 - iii) If the i/p frequency f_1 is reduced gradually, then the PLL will recapture the signal frequency at f_3 which is called as the upper edge of capture range & tracks it upto f_4 which is the lower edge of capture range & tracks it upto f_4 which is the lower edge of the lock range.
 - iv) Thus from PLL transfer curve of fig (b) we can write that.

$$f_3 - f_1 = \text{capture range}$$

$$f_2 - f_4 = \text{lock range.}$$

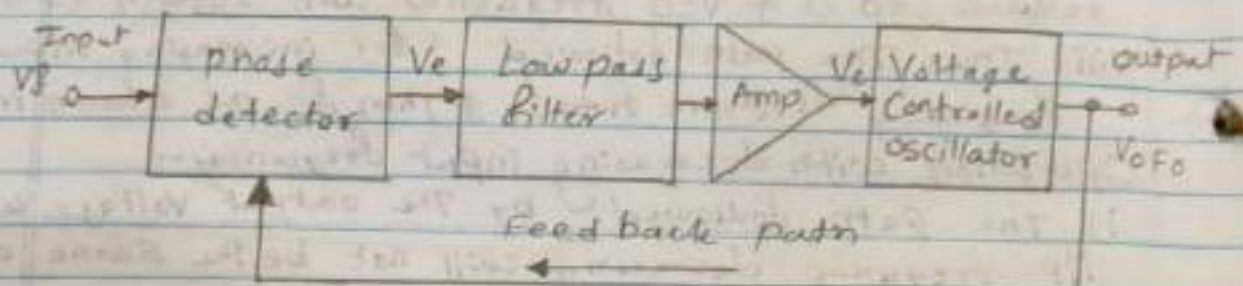
Application of PLL -

- (1) Frequency multiplication division
- (2) Frequency translation
- (3) Amplitude demodulation
- (4) Frequency demodulation
- (5) tracking Filters

Q.4 Define The block diagram of transfer curve for PLL & explain

Ans:- Block Diagram -

i) The PLL circuit is basically used for tracking a particular system



(b). A basic phase locked loop

- ii) It synchronizes its o/p with the i/p signal in terms of frequency & phase.
- iii) The state of synchronization betⁿ the input & output is called as the locked state. In the locked state the phase error betⁿ input & output is minimum.
- iv) If the error tries to creep in, then the PLL system will work automatically to minimize the phase error.
- v) Thus the phase of the output signal is locked to that of the input signal. Hence the name phase locked loop.
- vi) Block dia. of basic phase locked loop is as
- vii) As shown in this block diagram the phase locked loop consists of:

- 1) A phase detector or phase comparator
- 2) A low pass filter
- 3) An error amplifier
- 4) A voltage controlled oscillator (VCO)

Transfer characteristics —

- i) Fig (e) shows the transfer characteristics of PLL.
- ii) It is a graph of PLL output voltage V_F (plotted on the Y-axis) versus the frequency of the input signal i.e. f_i (plotted on X-axis)
- iii) The transfer characteristics indicates that the PLL exhibits the property of hysteresis like BH Curve.

Correctly

Siddhant College of Engineering
 Department of Mechanical Engineering
 Academic Year 2021-22, Semester I
 Subject: Heat & Mass Transfer 1020-92 Assessment Sheet

Roll No.	Name of the Student	Practical No. 1	Practical No. 2	Practical No. 3	Practical No. 4	Practical No. 5	Practical No. 6	Practical No. 7	Practical No. 8	Mark out of 80	Mark out of 25
72165753E	Abhishek Kumar Yadav	9	9	8	8	9	8	8	9	64	20
72165771M	Ajay Mohan Gowda	9	9	7	7	9	7	7	9	58	21
72165607H	ANRITA DALIYA KADAM	8	7	8	7	7	8	7	7	62	20
72165777L	Anant Dattora Jadhav	8	8	7	8	8	7	8	8	66	21
72165767C	Ashish Sangeet Deshmukh	9	9	8	7	9	8	7	9	67	21
72165717AL	Ashish Ramesh Mase	8	7	8	8	9	8	8	9	60	20
72165800E	Ashish Dattatray Wase	9	7	8	7	7	8	7	7	58	20
72165754M	Aniket Shivaji Sapat	7	7	8	7	7	8	7	7	62	20
72165755K	Anshu Gupta	7	8	8	7	8	8	7	8	64	21
72165763L	Anup H Chaudhari	8	8	8	8	8	8	8	8	64	20
72165756H	Ashodh Pravin Kawsarthi	8	8	8	8	8	8	8	8	68	20
72165760M	Arjun Yashwanth Dhole	9	7	7	9	7	7	7	7	58	20
72165812B	Ashvinih Tounekar	9	7	7	7	7	7	7	7	58	20
72165758D	Ashwini Chavhan	7	7	8	7	7	8	7	7	63	21
72165799B	Ashish Shankar Awghade	8	9	7	7	9	7	7	9	63	21
719139R2B	Aamresh Harishankar Satala	8	8	7	8	9	7	8	9	64	21
72165764F	Bhargav Babur Borga	7	9	9	8	9	7	8	9	64	21
71640636F	Dhanshraj Shankarshama Upadekar	8	8	8	8	8	8	8	8	62	20
72165773H	Dilip Ghure	8	8	7	8	8	7	8	8	62	20
72165769K	Disha Prashant Mandavro	8	9	8	7	9	8	7	9	65	21

Prin. Sagar Venkatesh Deshpande
 Subject Incharge

Dr. P. A. Mhasare
 H.O.D

Siddhant College of Engineering
Department of Mechanical Engineering
Academic Year 2021-22, Semester I
Subject: Heat & Mass Transfer 302042 Assessment Sheet

PRN	Name of The Student	Practical No. 1	Practical No. 2	Practical No. 3	Practical No. 4	Practical No. 5	Practical No. 6	Practical No. 7	Practical No. 8	Maximum Marks	Marks out of 80	Marks out of 25
72165753C	Gada Adesh Babubab	7	8	7	8	8	7	8	8	8	61	22
72165783E	Ganesh Teelidas Kumbhar	8	9	5	8	5	7	8	8	8	61	22
72165772K	Chare sagar vithal	9	7	8	8	8	7	8	8	8	60	22
72165791F	Jibendra Vasant Patil	7	7	7	7	7	8	7	7	7	57	20
72165775D	Krishna Gaytri	7	7	7	8	7	8	7	7	7	56	20
72165770C	Kundanashur Gokwad	9	8	8	7	7	8	8	7	7	58	20
72165765G	Susunhar deepak jadhav	9	8	3	8	8	8	7	8	8	63	20
72165784C	Madhav Tuladas Kumbhar	9	8	7	8	9	7	8	8	8	63	20
72165785M	Mano Trupti Jhendra	7	9	7	8	9	7	8	8	8	66	21
7209376C	Marech Umesh Moneya	8	7	8	8	7	7	8	8	8	64	20
72165781J	Mansi Kokate	9	8	8	8	8	8	8	8	8	61	22
72165779C	Mayur Pijpal Jadhav	9	8	7	8	8	8	8	8	8	65	20
7291972E	more prasad dharmaraj	7	7	7	8	7	7	8	8	8	61	20
72165780L	Magnack Bhavani Kumbhar	7	8	7	7	7	7	8	7	7	58	20
72165786K	Magru Nitin Soodar	8	11	7	7	8	7	7	7	7	58	20
72165787H	NARAYAN KALLAPPA KUMBHAR	8	8	8	8	8	8	8	8	8	60	20
721657810F	Nilesh Telgote	8	7	8	7	7	8	7	8	8	64	20
72165792D	Parashram Pandurang Patil	7	8	8	7	7	8	8	8	8	58	20
72165794L	Pawar Chandrakant Kulkarni	7	7	7	7	9	8	7	8	8	61	20
72165798J	Pawar Dadasaheb Nareskoti	7	9	7	8	7	7	7	7	7	58	20

Prof. Sagar Ashokrao Deshpande
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Dr. P. A. Maheswar
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Subharti College of Engineering
Department of Mechanical Engineering
Academic Year 2021-22, Semester I,
Subject: Heat & Mass Transfer 202042 Assessment Sheet.

PRN	Name of The Student	Practical No. 1	Practical No. 2	Practical No. 3	Practical No. 4	Practical No. 5	Practical No. 6	Practical No. 7	Practical No. 8	Maximum out of 80	Mark out of 25
72165764f	Pooja	9	0	0	0	9	0	0	9	00	25
72165813L	Prashantosh dipak wichare	9	9	0	7	9	7	9	9	64	21
72165805K	Pratik Shinkar	0	7	7	7	9	7	7	9	64	20
72165758c	Priyanka ramnesh suryawanhi	0	0	0	7	9	0	7	9	50	20
72165797E	Rahul B. Kamthar	0	0	7	0	9	0	7	9	61	21
71913948B	Rajkumar balasaheb dandinbar	9	9	0	7	9	7	9	9	69	23
72165799c	Rohit Sandeep sawant	0	0	0	0	9	0	0	9	67	21
72165788f	Rushikesh Pulchand Patkar	9	7	0	7	7	0	7	7	60	20
72165809B	Rushikesh sutar	7	7	0	7	7	0	7	7	58	20
72165766E	Ruturaj Deshmukh	7	0	0	7	0	0	7	7	61	20
72165782G	Sadhana shanting kshirsagar	0	0	0	0	0	0	0	0	64	21
72165799M	SAGAR JADHAV	0	0	0	0	0	0	0	0	64	20
72165800f	Saigraasad Nandkumar Shinde	0	7	7	7	7	7	7	7	58	20
72165793B	saniket patil	7	7	0	7	7	0	7	7	50	20
72165801G	Santosh Sarjano Gade	0	9	7	7	9	0	7	9	58	20
72165803C	SATHE DEEPAANILAY DNYANESHWAR	0	0	7	0	9	7	7	9	63	21
72165789D	Sayali Bajirao Paraskar	7	0	7	0	9	7	0	9	64	21
72165804M	shahil jawar	0	0	0	0	0	0	0	0	64	21
71826250c	Shinde Ganesh balaso	0	0	7	0	0	7	0	0	62	20
72165776B	Shreshth Hirakot	0	0	0	7	9	0	7	9	63	21
72165806H	Shubham Jagdish takhate	9	7	9	7	7	7	7	7	58	20
72165778f	Shubham Rajendra Jadhav	7	7	0	7	7	0	7	7	58	20
72165807F	Shubham rajendra patil	0	9	7	7	9	7	7	9	63	21
72165808D	Siddesh Karthik Jadhav	0	9	7	0	9	7	0	9	65	22
71826272H	Sunil Haribhau Manale	7	9	7	0	9	7	0	9	64	21
71826141M	Umesh Jilgude	0	0	0	0	0	0	0	0	64	21
72165790H	vivek Pandey	0	0	7	0	0	7	0	0	62	20
72165815C	Yashu Ranjan Mujawar	0	0	0	7	9	0	7	0	65	21

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