CAYMET's

Siddhant College of Engineering

Academic Calendar

(A.Y. 2021-2022) Semester –I

Date:-03/08/2021

Sr. No	Activity	Proposed Dates
1.	Commencement of Teaching (TE & BE) (SEM-I).	15th June 2021.
2.	Internal Academic & Administrative Audit.	Third week of June 2021.
3.	World Yoga Day Celebration [Online].	21st June 2021.
4.	Bakri - Id (Id-Ul-Zua).	21st July 2021.
5.	Independence Day.	15th August 2021.
6.	Parsi New Year (Shahenshahi).	16th August 2021.
7.	Moharum.	19th August 2021.
8.	Commencement of Teaching (SE & ME II Year) (SEM-I).	20th August 2021.
9.	IQAC Meeting – I [Online].	27th August 2021.
10.	Departmental In-sem Exam (TE, BE & ME II Year) [Online MCQ's Type] -30 Marks.	Last week of August 2021.
11.	Declaration of Departmental In-sem Exam (TE, BE & ME- II Year) Result.	1st September 2021.
12.	Celebration of SGI Foundation Day.	1st September 2021.
13.	Celebration of Teachers Day.	5th September 2021.
14.	Ganesh Chaturthi.	10th September 2021.
15.	Celebration of Engineers Day.	15th September 2021.
16.	Mahatma Gandhi Jayanti	2nd October 2021.
17.	Commencement of FE & FE Induction programme (SEM-I).	First and Second week of October 2021.
18.	Department wise Prelim Exam (TE, BE & ME II Year) [Online MCQ's Type]-50 Marks.	First week of October 2021.
19.	Declaration of Departmental Prelim Exam Result.	11th October 2021.
20.	Department wise Practical Conduction of UG & PG [Online].	Second week of October 2021.
21	Commencement of ME I Year. Induction programme of ME I Year & Direct Second Year students (SEM-I).	Second week of October 2021.
22.	End Term Submission (TE & BE).	Second week of October 2021.
23.	Dasara	15th October 2021.
24.	Id-E-Milad.	19th October 2021.
25.	End of Semester I (TE & BE).	20th October 2021.
26.	Departmental In-sem Exam of FE, SE & ME I	Last week of October 2021.

Siddhant College of Engineering, Sudumbare, Pune- 412109 SEAL

	Year [Online MCQ's Type] -30 Marks.	
27.	Commencement of vacation for staff.	Last week of October 2021.
28.	SPPU Practical / Oral Examination (TE & BE) [Online]	Last week of October 2021.
29.	SPPU Theory Examination (TE & BE) [Online].	First week of November 2021.
30.	Declaration of Departmental In-sem Exam (FE, SE, ME- I & II Year) Result.	3rd November 2021.
31.	Diwali Amavasaya – Lakshmi Pujan.	4th November 2021.
32.	Diwali-Bali Pratipada	5th November 2021.
33.	Diwali-Bhaubeej	6th November 2021.
34.	Parent Teacher Meet [Online].	8th November 2021.
35.	Department wise Prelim Exam (SE & ME II Year) [Online MCQ's Type]-50 Marks.	Second week of November 2021.
36.	End Term Submission (SE & ME II Year).	Second week of November 2021.
37.	End of Semester I (SE & ME II Year).	12th November 2021.
38.	Declaration of Departmental Prelim Exam (SE & ME II Year) Result.	12th November 2021.
39.	Gurunanak Jayanti.	19th November 2021.
40.	IQAC Meeting – II [Online].	26th November 2021.
41.	NAAC-AQAR Data filling for last academic year.	First week of December 2021.
42.	FE & ME I Year Prelim Exam [Online MCQ's Type]-50 Marks.	First week of December 2021.
43.	End Term Submission (FE & ME I Year) & Prelim Results.	Second week of December 2021.
44.	End of Semester I (FE & ME I Year).	10th December 2021.
45.	SPPU Practical / Oral Examination (FE, SE, ME-I & II Year) [Online]	Third week of December 2021.
46.	Christmas.	25th December 2021.
47.	SPPU Theory Examination (FE, SE, ME- I & II Year) [Online].	Last week of December 2021.

- Monthly Defaulter list-End of Every month during academic period.
- HOD Meeting with Faculty-Every Thursday.
- Principal Meeting with HoD-Every Friday.
- T&P activity-Every Thursday & Friday /as per the schedule given by T&P coordinator.
- NSS Activity-2 activities per semester.

Siddhant College of Engineering • Sudumbare Pune- 412109 • SEAL

Prof. M. V. Shinde
Principal

Principal
Siddhant College of Engineering
Sudumbare, Pune - 412 109

CAYMET's

Siddhant College of Engineering

Academic Calendar

(A.Y. 2021-2022) Semester –II

Date:-28/12/2021

Sr. No	Activity	Proposed Dates
1.	Commencement of Teaching (TE & BE) (SEM-II).	15th November 2021.
2.	Departmental In-sem Exam (TE & BE) [Online MCQ's Type] -30 Marks.	Last week of December 2021.
3.	Declaration of In-sem Exam Result (TE & BE).	3rd January 2022.
4.	Commencement of Teaching (SE & ME II Year) (SEM-II).	3rd January 2022.
5.	Commencement of (FE & ME I Year) and FE Induction programme (SEM-II).	Second week of January 2022.
6.	Republic Day.	26th January 2022.
7.	College level SPPU Convocation Ceremony [Online].	First week of February 2022.
8.	E-Alumni Meet.	First week of February 2022.
9.	Chhatrpati Shivaji Maharaj Jayanti.	19th February 2022.
10.	IQAC Meeting-III [Online].	25th February 2022.
11.	Departmental In-sem Exam (FE, SE, ME I & II Year) [Online MCQ's Type] -30 Marks.	Last week of February 2022.
12.	Mahashivratri.	1st March-2022.
13.	Declaration of In-sem Exam Result (FE, SE, ME I & II Year).	3rd March 2022.
14.	Department wise Practical Conduction of UG & PG [Online].	Second week of March 2022.
15.	Holi [Second Day].	18th March 2022.
16.	Gudhi Padwa	2nd April 2022.
17.	Ram Navami.	10th April 2022.
18.	Department wise Prelim Exam [Online MCQ's Type]-50 Marks (TE & BE).	Third week of April 2022.
19.	Dr. Babasaheb Ambedkar Jayanti.	14th April 2022.
20.	Good Friday.	15th April 2022.
21.	End Term Submission (TE & BE) & Prelim Results.	Last week of April 2022.
22.	Feedback Analysis [Online].	28th April 2022.
23.	Parent Teacher Meet [Online].	29th April 2022.
24.	End of Semester (TE & BE).	30th April 2022.
25.	Maharashtra Din.	1st May 2022.
26.	SPPU Practical / Oral Examination (TE & BE). [Online]	First Week of May 2022.

Siddhant College of Engineering SEAL Sudumbare Pune-412109

27.	Commencement of Remedial Classes [Online].	2nd May 2022.
28.	Ramzan –Id [Id-Ul-Fitr].	3rd May 2022.
29.	Department wise Prelim Exam [Online MCQ's Type]-50 Marks (FE,SE, ME I & II Year)	First week of May 2022.
30	End Term Submission (FE, SE, ME I & II Year) & Prelim Results.	Second week of May 2022.
31.	SPPU Theory Examination (TE & BE) [Online].	Second week of May 2022.
32.	End of Semester (FE, SE, ME I & II Year).	15th May 2022.
33.	Commencement of vacation for Staff.	15th May 2022.
34.	Buddha Pournima	16th May 2022.
35.	SPPU Practical / Oral Examination (FE, SE, ME I & II Year) [Online].	Third week of May 2022.
36.	SPPU Theory Examination (FE, SE, ME I & II Year) [Online].	Last week of May 2022.
37.	IQAC Meeting-IV [Online].	27th May 2022.
38.	Commencement of vacation for Students.	31st May 2022.

- Monthly Defaulter list-End of Every month during academic period.
- HOD Meeting with Faculty-Every Thursday.
- Principal Meeting with HoD-Every Friday.
- T&P activity-Every Thursday & Friday /as per the schedule given by T&P coordinator.
- NSS Activity-2 activities per semester.

Siddhant College of Engineering Sudumbare, Pune, 412109 SEAL

Prof. U. V. Shinde
Principal
Siddhant College of Engineering
Sudumbare, Pune - 412 109

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING

DEPARTMENT OF MECHANICAL ENGINEERING

Master Time Table of Mechanical Department For Online Lecture , AY 2021-22, Semester – I, w. e. f. 20/10/2021

Day	Year & Div.	09.30-10.30	10.30-11.30	11.30-12.30	12:30-01.30	01:30-02.30	02.30-03.30	03.30-04.30
Monday	SE – A	EM&M(GGS)	SM&D (F1)	SM(SIB)	Lunch Break	ET(VSM)	EEE (SRG)	
	TE – A	NSM(PPG)	ELEC-I AFJP(BDG)	DME (Dr.PAM)		MTX (F2)	HT (SUD)	H&M- Robotics/EV-PPG
	BE – A	ELEC-I HVAC/FEA (VSM/SUD)	DOM(RRK)	H&P(GGS)		ELEC-II AE/EAM (PPG/ F2)	CAD CAM(BBK)	
Tuesday	SE – A	EM&M (GGS)	SM&D (F1)	SM(SIB)	Lunch Break	ET(VSM)	EEE(SRG)	
	TE – A	NSM (PPG)	ELEC-I AFJP(BDG)	DME (Dr.PAM)		MTX (F2)	HT (SUD)	H&M- Robotics/EV-PPG
	BE – A	ELEC-I HVAC/FEA (VSM/SUD)	DOM(RRK)	H&P (GGS)		ELEC-II AE/EAM (PPG/F2)	CAD CAM (BBK)	
Wednesday	SE – A	EM&M (GGS)	SM&D (F1)	SM(SIB)	Lunch Break	ET(VSM)	EEE (SRG)	
	TE – A	NSM (PPG)	ELEC-I AFJP(BDG)	DME (Dr.PAM)		MTX (F2)	HT (SUD)	H&M- Robotics/EV-PPG
	BE – A	ELEC-I HVAC/FEA (VSM/SUD)	DOM(RRK)	H&P(GGS)		ELEC-II AE/EAM (PPG /F2)	CAD CAM (BBK)	
Thursday	SE – A	EM&M (GGS)	SM&D (F1)	SM(SIB)	Lunch Break	ET(VSM)	EEE (SRG)	
	TE – A	NSM (PPG)	ELEC-I AFJP(BDG)	DME (Dr.PAM)		MTX (F2)	HT (SUD)	H&M- Robotics/EV-PPG
	BE – A	ELEC-I HVAC/FEA (VSM/SUD)	DOM(RRK)	H&P(GGS)		ELEC-II AE/EAM (PPG/)	CAD CAM (BBK)	
Friday	SE – A	EM&M(GGS)	SM&D (F1)	SM(SIB)	Lunch Break	ET(VSM)	EEE(SRG)	
	TE – A	NSM(BBK)	ELEC-I AFJP(BDG)	DME (Dr.PAM)		MTX (F2)	HT (SUD)	H&M- Robotics/EV-PPG
	BE – A	Project Work-I						

Class-Teacher & Batch-Wise GFM

Year - Div.	Class Teacher	Batch	GFM	Batch	GFM	Batch	GFM
SE-A	SIB	A1	Prof. S.I. Bharadiya	A2	Prof. G.G.Singh	A3	F2
TE-A	PPG	A1	Prof. P.P.Gedam	A2	Prof. B.D.Garje	A3	Prof. S.U.Deshpande
BE-A	VSM	A1	Prof. V.S.Munde	A2	F1	A3	Prof.S.S.Kedar

 # TE ELECTIVE I: -1) Advanced Forming & Joining Processes

 # TE Honors & Minors: -

1) Robotics
2) Electric Vehicle

 # BE ELECTIVE I: -

1)Finite Element Analysis
2)Heating Ventilation and Air Conditioning

 # BE ELECTIVE II: -

1)Automobile Engineering
2)Energy Audit and Management

Departmental Time Table Incharge

HOD Mechanical

Principal

CAYMET's
SIDDHANT COLLEGE OF ENGINEERING
DEPARTMENT OF MECHANICAL ENGINEERING
MASTER TIME TABLE (MECH) SEM- II, 2021-22

DAY	CLASS/DIV	8:40-9:40	9:40-10:40	10:40-11:00	11:00-12:00	12:00-01:00	01:00-01:30	01:30-02:30	02:30-03:30	03:30-04:30
Monday	SE	AT (VSM)	LIB HR.	SHORT RECESS	A1-LIB A2-EM III (FT) A3-M/D (SDG)		LONG RECESS	EDM (BRK)	A1- EM III (FT), A2- AT (VSM), A3-KDM (BRK)	
	TE	DTS (PAM)	CAE (BRK)		A1-DTS (PAM) A2-CAE (BRK) A3-AT & ME (PPC)			LIB HR	TNP HOUR(Skill development program)	
	BE	EE (SUD)	ELE -III ROBOTICS/IE (PPG/SGD)		G.S.-IV AMP (SVC)	HSD (SIB)		ELE.-III ROBOTICS/IE (PPG/SGD)	A1-EE (SUD) A2- LIB HR/EB A3-MSD (PAM)	
Tuesday	SE	MP (GGD)	AT (VSM)		EM-III (FT)	EM-III (FT)		EDM (BRK)	A1- EDM (BRK), A2- MS (BDG), A3- FM (PPG)	
	TE	ELEC-II (CM/SE) SG & BDG	DTS (PAM)		AI & ML (PPC)	ELEC-II (CM/SE) SG & BDG		A1- CAE (BRK) A2- AI & ML (PPC) A3-ML (SG)		GPM HOUR
	BE	ELE.-IV AMP (SVC)	EE (SUD)		ELE.-III ROBOTICS/IE (PPG/SGD)	ELE.-IV AMP (SVC)		MSD (SIB)	A1-LIB A2-Project A3-LIB HR/EB LIB	
Wednesday	SE	LIB HR.	AT (VSM)		A1- MS (BDG) A2- KDM (BRK) A3 - LIB			SUBJECT LECTURES		
	TE	CAE (BRK)	AI & ML (PPC)		A1-FP & CLAB (VSM) A2-LIB A3-DTS (PAM)			ELEC-II (CM/SE) SG & BDG	TNP HOUR(Skill development program)	
	BE	A1-Project, A2-LIB, A3-ELE -III (PPG/GGD)			LIB HR.	MSD (SIB)		A1-MSD (SIB) A2-ELE -III (PPG/GGD) A3-LIB		EE (SUD)
Thursday	SE	FM (PPG)	MP (GGD)		EM-III (FT)	AT (VSM)		EDM (BRK)	MP (GGD)	LIB HR
	TE	DTS (PAM)	AI & ML (PPC)		LIB HR.	CAE(BRK)		A1-ME(SG), A2- FP & C LAB (VSM), A3-LIB HR.		GPM HOUR
	BE	MSD (SIB)	LIB HR.		A1-ELE -III (PPG/GGD), A2-MSD (SIB), A3-EE (SUD)			A1- LIB HR/EB LIB A2-EE (SUD) A3- PROJECT		ELE.-IV ROBOTICS/VE (PPG/GGD)
Friday	SE	EM-III (FT)	FM (PPG)		A1-FM (PPG) A2- LIB,A3 - AT (VSM)			FM (PPG)	A1-AT (VSM), A2-FM (PPG),A3-EM III (FT)	
	TE	A1- LIB ,A2-ML (SG),A3-FP & CLAB (VSM)			A1-AI &ML (PPC), A2-DTS (PAM) A3-CAE (BRK)			CAE (BRK)	TNP HOUR(Skill development program)	
	BE	PROJECT			PROJECT			PROJECT		SPORTS HOUR
Saturday	SE	PROJECT &AMID LEARNING			PROJECT BASED LEARNING			INDUSTRIAL VISIT		
	TE	INTERNSHIP / MINI PROJECT			INTERNSHIP / MINI PROJECT			INDUSTRIAL VISIT		
	BE	INDUSTRIAL VISIT			INDUSTRIAL VISIT			INDUSTRIAL VISIT		

Year	Class Teacher
SE (Class Room-IOT Lab)	Prof. C.D. Singh
TE (Class Room-A-10)	Prof. R.D. Dange
BE (Class Room- A-11)	Prof. S.U. Deshpande

CLASS	Batch	GPM	Batch	GPM	Batch	GPM
SE	A1	GDS	A2	VSM	A3	PPG
TE	A1	BDG	A2	PPC	A3	SG
BE	A1	SUD	A2	SIB	A3	VC

Prof. P.P.Gedam & Prof.S.V.Chambhare
Departmental Time Table Incharge

Dr. P. J. Mahesare
HOD Mechanical

Dr. R. L. Khandagale
Principal

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE, PUNE

Department of Electronics &Telecommunication

Academic Year: 2021-2022 **Semester: - VII**

Class: BE (E & TC)

Class Teacher: Prof. A. A. Kokate

CLASS TIME TABLE

w.e.f.15 /07/2021

DAY / TIME	8.45 - 9.45	9.45- 10:45	10:45 - 11.00	11.00- 12.00	12.00- 1.00	1.00- 1.30	1.30- 2.30	2.30- 3.30	3.30- 4.30
MON	CNS (SVP)	VLSI (AAK)	SHORT BREAK	EPD (NUK)	ERTOS (AVB)	LONG BREAK	RMT (VSB)	CNS(A1)(SVP)	
TUE	ERTOS (AVB)	CNS (SVP)		RMT (VSB)	EPD (NUK)		VLSI (AAK)	VLSI(A1)(AAK)	
WED	RMT (VSB)	EPD (NUK)		VLSI (AAK)	CNS (SVP)		ERTOS (AVB)	RMT(A1)(VSB)	
THU	RMT (VSB)	CNS (SVP)		VLSI (AAK)	ERTOS (AVB)		EPD (NUK)	ERTOS (A1)(AVB)	
FRI	VLSI (AAK	CNS (SVP)		ERTOS (AVB)	RMT (VSB)		EPD (NUK)	TNP/INDUSTRIAL VISIT	

Theory	
Subject	Name of the Teacher
EPD	NUK-Prof. N.U. Kure
ERTOS	AVB- Prof. Ashwini Bade
CNS	SVP- Prof. S.V. Patil
RMT	VSB-- Prof. V.S. Bhatlawande
VLSI	AAK-Prof. A. A. Kokate

Practical/Tutorial		
Subject	Name of the Laboratory	Name of the Teacher
ERTOS	SPECIALISATION LAB	AVB- Prof. Ashwini Bade
CNS	RESEARCH SPECIALISATION LAB	SVP- Prof. S.V. Patil
RMT	INSTRUMENTATION LAB	VSB-- Prof. V.S. Bhatlawande
VLSI	RESEARCH SPECIALIZATION LAB	AAK-Prof. A. A. Kokate

Prof. Ashwini A. Kokate
TIME TABLE CO-ORDINATOR

Prof. Ashwini Bade
H.O.D (E&TC)

Prof. [illegible] V.Shinde
PRINCIPAL

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE, PUNE

Department of Electronics &Telecommunication

Academic Year: 2021-2022

Semester: -

Class: SE III

Class Teacher: Prof. Prabhat Pallav

CLASS TIME TABLE

w.e.f. 15/07/2021

DAY / TIME	8.45 - 9.45	9.45-10:45	10:45 - 11.00	11.00 - 1.00	1.00-1.30	1.30-2.30	2.30-3.30	3.30-4.30
MON	M-III (AT)	Elex-C (PP)	BREAK	Elex-C (A1)(PP)	BREAK	DC (NUK)	Elect-C ( )	ESD ( )
TUE	Elex-C (PP)	DC (NUK)		DS (A1)(VSB)		DS (VSB)	M-III (AT)	Elect-C ( )
WED	DC (NUK)	Elex-C (PP)		Elect-C(A1) ( )		DS (VSB)	Elect-C ( )	M-III (AT)
THU	Elex-C (PP)	DS (VSB)	SHORT	EMIT(A1)(AP)	LONG	Elect-C ( )	M-III (AT)	ESD ( )
FRI	Elect-C ( )	DC (NUK)		DC(A1)(NUK)		DS (VSB)	Elex-C (PP)	M-III (AT)

Theory		Practical/Tutorial		
Subject	Name of the Teacher	Subject	Name of the Laboratory	Name of the Teacher
M-III	AT- Prof. A. Takale			
Elex-C	PP-Prof. Prabhat Pallav	DC	DE LAB	NUK - Prof. N. U. Kure
Elect-C		Elect-C	SSDC LAB	
DC	NUK - Prof. N. U. Kure	DS	Software LAB	VSB-- Prof. V.S. Bhatlawande
DS	VSB-- Prof. V.S. Bhatlawande	Elex-C	BASIC ELECTRIC LAB	
ESD		ESD	INSTRUMENTATION LAB	

Prof. Ashwini A. Kokate
TIME TABLE CO-ORDINATOR

Prof. Ashwini Bade
H.O.D (E&TC)

Prof. [illegible] V.Shinde
PRINCIPAL

SIDDHANT COLLEGE OF ENGINEERING,SUDUMBARE,PUNE

Department of Electronics &Telecommunication

Academic Year: 2021-2022 **Semester: - V**

Class: TE

Class Teacher: Prof. N. U. Kure

CLASS TIME TABLE

w.e.f. 15/07/2021

DAY / TIME	8.45 - 9.45	9.45-10.45	10:45 - 11.00	11.00 - 1.00	1.00-1.30	1.30-2.30	2.30-3.30	3.30-4.30
MON	CN (PP)	EFT (NUK)	SHORT BREAK	DSP(A1)(AAK)	LONG BREAK	MC (AVB)	DBMS (AAK)	DC (SVP)
TUE	DBMS (AAK)	CN (PP)		ESD(A1)(NSK)		MECT(A1)(AVB)		EFT (NUK)
WED	DC (SVP)	MC (AVB)		MC(A1)(AVB)		EFT (NUK)	CN (PP)	DBMS (AAK)
THU	EFT (NUK)	DBMS (AAK)		EMTL(A1)(NUK)		MC (AVB)	DC (SVP)	CN (PP)
FRI	EFT (NUK)	MC (AVB)		DC(A1)(SVP)		DBMS (AAK)	DC (SVP)	SD

Theory	
Subject	Name of the Teacher
EFT	NUK - Prof. N. U. Kure
MC	AVB -Prof. A. V. Bade
DC	SVP- Prof. S.V. Patil
DBMS	AAK- Prof A. A. Kokate
CN	PP-Prof. Prabhat Pallav
SD	

Practical/Tutorial		
Subject	Name of the laboratory	Name of the Teacher
CN	SPECIALIZATION LAB	PP-Prof. Prabhat Pallav
MC	MCA LAB	AVB -Prof. A. V. Bade
DC	COMN LAB	SVP- Prof. S.V. Patil
DBMS	RESEARCH SPECIALIZATION LAB	AAK- Prof. A. A. Kokate
EMTL	B. ELECTRICAL LAB	NUK - Prof. N. U. Kure

Prof. Ashwini A. Kokate
TIME TABLE CO-ORDINATOR

Prof. Ashwini Bade
H.O.D (E&TC)

Prof. U. V. Shinde
PRINCIPAL

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE, PUNE

Department of Electronics &Telecommunication

Academic Year: 2021-2022 **Semester: - I**

Class: ME FE (VLSI & EMBEDDED SYSTEMS)

Class Teacher: Prof. M.U Inamdar

CLASS TIME TABLE

w.e.f. 1/08/2021

DAY / TIME	8.30 - 9.25	9.25-10:20	10:20 - 10.50	10.50-11.45	11.45-12.40	12.40-1.30	1.30-2.25	2.25-3.20	3.20-4.15
MON	RM (SVP)		BREAK	RM (SVP)	WSN (VSB)	BREAK		RM(A1)(SVP)	
TUE	RM (SVP)	D-CMOS (JRP)		WSN (VSB)	ESD (AVB)		D-CMOS (JRP)	D-CMOS(A1)(JRP)	
WED	RC (NSK)	RC (NSK)		ESD (AVB)	D-CMOS (JRP)		RM (SVP)	RC(A1)(NSK)	
THU	WSN (VSB)	WSN (VSB)	SHORT	D-CMOS (JRP)	RC (NSK)	LONG	WSN (A1)(VSB)		
FRI	ESD (AVB)	ESD (AVB)		RC (NSK)			ESD(A1)(AVB)		WNS (VSB)

Theory	
Subject	Name of the Teacher
RC	NSK- Prof. N.S. Kulkarni
WSN	VSB- Prof. V.S. Bhatlawande
ESD	AVB - Prof. A. V. Bade
RM	SVP- Prof. S.V. Patil
D-CMOS	JRP- DR. J. R. Panchal

Practical/Tutorial		
Subject	Name of the Laboratory	Name of the Teacher
RC	RESEARCH SPECIALIZATION LAB	NSK- Prof. N.S. Kulkarni
WSN	SPECIALIZATION LAB	VSB- Prof. V.S. Bhatlawande
ESD	MCA LAB	AVB - Prof. A. V. Bade
RM	RESEARCH SPECIALIZATION LAB	SVP- Prof. S.V. Patil
D-CMOS	RESEARCH SPECIALIZATION LAB	JRP- DR. J. R. Panchal

Prof. Ashwini A. Kokate
TIME TABLE CO-ORDINATOR

Prof. Ashwini Bade
H.O.D (E&TC)

Prof. U. V. Shinde
PRINCIPAL

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE, PUNE

Department of Electronics &Telecommunication

Academic Year: 2021-2022 Semester: - III

Class: ME (VLSI & EMBEDDED SYSTEMS)

CLASS TIME TABLE

w.e.f. 1 / 8 /2021

DAY / TIME	8.30 - 9.25	9.25-10:20	10:20 - 10.50	10.50-11.45	11.45-12.40	12.40 -1.30	1.30-2.25	2.25-3.20	3.20-4.15
MON			BREAK			BREAK			
TUE									
WED									
THU	TVVC (AAK)	ELCT-III(VSB)	SHORT	ELCT-III(VSB)	TVVC (AAK)	LONG	SEM-II	TVVC(A1)(AAK)	
FRI	ASIC (NSK)	ASIC (NSK)		TVVC (AAK)	TVVC (AAK)		SEM-II	ASIC(A1)(NSK)	
SAT	ELCT-III(VSB)	ELCT-III(VSB)		ASIC (NSK)	ASIC (NSK)		ELCT-III(A1)(VSB)		

Theory		Practical/Tutorial		
Subject	Name of the Teacher	Subject	Name of the Laboratory	Name of the Teacher
ELCT-III	VSB- Prof. V.S. Bhatlawande	ELCT-III	RESEARCH SPECIALIZATION LAB	VSB- Prof. V.S. Bhatlawande
ASIC	NSK- Prof. N.S. Kulkarni	ASIC	RESEARCH SPECIALIZATION LAB	NSK- Prof. N.S. Kulkarni
TVVC	AAK- Prof A. A. Kokate	TVVC	RESEARCH SPECIALIZATION LAB	AAK- Prof A. A. Kokate

Prof. Ashwini A. Kokate
TIME TABLE CO-ORDINATOR

Prof. Ashwini Bade
H.O.D (E&TC)

Prof. U.V.Shinde
PRINCIPAL

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF _____ ENGINEERING

MASTER TIME-TABLE

SEM II

A.Y.:-2021-22

WITH EFFECT FROM :

DAY / TIME	MONDAY					TUESDAY					WEDNESDAY					THURSDAY					FRIDAY		
	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE
9:45 - 9:45	SS (SBD)	CN (GAA)	BCS (PP)	SOC (NUK)		CS (SVS)	PM (KAK)	MC (GAA)	SOC (NUK)		SS (SBD)	PDC (NUK)	MC (GAA)			CS (SVS)	CN (GAA)	WSN (SBD)	SOC (NUK)		SS (SBD)	PDC (NUK)	MC (GAA)
9:45 - 10:45	POCS (KAK)	EP (AVB)	WSN (SBD)	ACMOS (AVB)		ESD (SVS)	EP (AVB)	WSN (SBD)	ACMOS (AVB)		OOP (AVB)	PDC (NUK)	MC (GAA)	ACMOS (AVB)		OOP (AVB)	CN (GAA)	BCS(PP)	S (AVB)		OOP (AVB)	PDC (NUK)	MC (GAA)
10:45 - 11:00	SHORT BREAK																						
11:00- 12:00	CS (SVS)	PDC (NUK)	AVE (VSB)			POCS (KAK)	PDC (NUK)	BCS (PP)	EAS (VSB)		CS (SVS)	MC (GAA)	BCS(PP)	EAS (VSB)		POCS (KAK)	PDC (NUK)	AVE (VSB)			DAL	PM (KAK)	BCS (PP)
12:00- 01:00	ESD (SVS)	EP (AVB)	MC (GAA)	EAS (VSB)		ESD (SVS)	CN (GAA)	AVE (VSB)			CS (SVS)	PROJE CT	AVE (VSB)			DAL	PROJE CT	MC (GAA)	EAS (VSB)		DAL	PROJE CT	AVE (VSB)
1:00 - 1:30	LUNCH BREAK																						
1:30 - 2:30	SS (SBD)	EP (AVB)	BCS (PP)	SOC (NUK)		PBL	PDC (NUK)	BCS(PP)			POCS (KAK)	LIB	BCS(PP)			CS (SVS)	CN (GAA)	AVE(VSB)	EPD (PP)		ESD (SVS)	LIB	AVE(V SB)
2:30-3:30	SS (SBD)	TNP	AVE (VSB)	EPD (PP)		PBL	PDC (NUK)	PS2			POCS (KAK)	TNP	PS2			CS (SVS)	CN (GAA)	PS2			ESD (SVS)	TNP	LIB
3:30-4:30	SS (SBD)	TNP	PS2			PBL	PDC (NUK)	LIB	EPD (PP)		POCS (KAK)	TNP	LIB	EPD (PP)		CS (SVS)	CN (GAA)	LIB	EPD (PP)		ESD (SVS)	TNP	LIB

Time Table In-charge
Prof. Kalyani Kadam

Time table Coordinator
Prof. Kalyani Kadam

HOD
Prof. Prabhat Pallav

Principal
Dr. Rahul Khandagale

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF _E&TC_ ENGINEERING

MASTER TIME-TABLE

Name of Staff: Prof. Ashwini Badle

A.Y. 2023-24

DAY / TIME	MONDAY					TUESDAY					WEDNESDAY					THURSDAY					FRIDAY				
	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II
9:40 - 9:45																									
9:45 - 10:40		EP (AVB)		ACMOS			EP (AVB)		ACMOS		OOP (AVB)			ACMOS		OOP (AVB)			ACMOS		OOP (AVB)				
10:40 - 11:00	SHORT BREAK																								
11:00- 12:00																									
12:00- 01:00		EP (AVB)										MINI PROJECT	AVE (VSB)				MINI PROJECT					MINI PROJECT			
1:00 - 1:30	LUNCH BREAK																								
1:30 - 2:30		EP (AVB)																							
2:30-3:30								PS2					PS2					PS2							
3:30-4:30			PS2																						

Time Table In-charge
Prof. Kalyani Kadam

Time table Coordinator
Prof. Kalyani Kadam

HOD
Prof. Prabhat Pallav

Principal
Dr. Rahul Khandagale

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF _E&TC_ ENGINEERING

MASTER TIME-TABLE

Name of Staff: Prof. Vallabh Bhatlawande A.Y.:2021-22 SEM II WITH EFFECT FROM :

DAY / TIME	MONDAY					TUESDAY					WEDNESDAY					THURSDAY					FRIDAY		
	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE
9:40 - 9:45																							
9:45 - 10:45																							
10:45 - 11:00	SHORT BREAK																						
11:00- 12:00			AVE (VSB)						EAS (VSB)					EAS (VSB)				AVE (VSB)				
12:00- 01:00				EAS (VSB)				AVE (VSB)				MINI PROJECT	AVE (VSB)				MINI PROJECT		EAS (VSB)			MINI PROJECT	AVE (VSB)
1:00 - 1:30	LUNCH BREAK																						
1:30 - 2:30																		AVE(VSB)					AVE(VSB)
2:30-3:30			AVE (VSB)					PS2					PS2					PS2					
3:30-4:30			PS2																				

Time Table In-charge
Prof. Kalyani Kadam

Time table Coordinator
Prof. Kalyani Kadam

HOD
Prof. Prabhat Pallar

Principal
Dr. Rahul Khaudagale

CsVMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF _____ ENGINEERING

MASTER TIME-TABLE

Name Of Staff: Prof. Namita Kure

AY: 2021-22 | SEM: II | WITH EFFECT FROM:

DAY / TIME	MONDAY					TUESDAY					WEDNESDAY					THURSDAY					FRIDAY				
	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II
9:45 - 9:45				SOC (NUK)					SOC (NUK)			PDC (NUK)							SOC (NUK)			PDC (NUK)			
9:45 - 10:45												PDC (NUK)										PDC (NUK)			
10:45 - 11:00	SHORT BREAK																								
11:00- 12:00		PDC (NUK)					PDC (NUK)										PDC (NUK)								
12:00- 13:00												MINI PROJE CT					MINI PROJE CT					MINI PROJE CT			
1:00 - 1:30	LUNCH BREAK																								
1:30 - 2:30				SOC (NUK)			PDC (NUK)																		
2:30-3:30							PDC (NUK)	PS2					PS2					PS2							
3:30-4:30			PS2				PDC (NUK)																		

Time Table In-charge
Prof. Kalyani Kadam

Time table Coordinator
Prof. Kalyani Kadam

HOD
Prof. Pritikan Patil

Principal
Dr. Rahul Khawlagale

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF __E&TC_ ENGINEERING

MASTER TIME-TABLE

A.Y. 2021-22

Name Of Staff: Prof. Prabhat Pallav

DAY / TIME	MONDAY					TUESDAY					WEDNESDAY					THURSDAY					FRIDAY				
	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II	SE	TE	BE	ME I	ME II
9:40 - 10:40			BCS (PP)																						
10:40 - 11:40																		BCS(PP)							
11:40 - 12:40	SHORT BREAK																								
12:40- 01:40								BCS (PP)					BCS(PP)												BCS (PP)
1:40 - 2:30												MINI PROJECT					MINI PROJECT					MINI PROJECT		
2:30 - 3:30	LUNCH BREAK																								
3:30 - 4:30			BCS (PP)					BCS(PP)					BCS(PP)							EPD (PP)					
4:30-5:30				EPD (PP)				PS2					PS2					PS2								
5:30-6:30			PS2						EPD (PP)					EPD (PP)						EPD (PP)					

Time Table In-charge
Prof. Kalyani Kadam

Time table Coordinator
Prof. Kalyani Kadam

HOD
Prof. Prabhat Pallav

Principal
Dr. Rahul Khandagale

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF E&TC ENGINEERING

MASTER TIME-TABLE

Name Of Staff: Prof. Swati Deshmukh

A.Y.-2021-22 SEM II WITH EFFECT FROM :

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
8:45 - 9:45	SS (SBD)						SS (SBD)					WSN (SBD)	SS (SBD)		
9:45 - 10:45			WSN (SBD)			WSN (SBD)									
10:45 - 11:00	SHORT BREAK														
11:00- 12:00													DAL		
12:00- 01:00								MINI PROJE CT		DAL	MINI PROJE CT		DAL	MINI PROJE CT	
1:00 - 1:30	LUNCH BREAK														
1:30 - 2:30	SS (SBD)														
2:30-3:30	SS (SBD)														
3:30-4:30	SS (SBD)														

Time Table In-charge
Prof. Kalyani Kadam

Time table Coordinator
Prof. Kalyani Kadam

HOD
Prof. Prabhat Pallav

Principal
Dr. Rahul Khandagale

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF E&TC ENGINEERING

MASTER TIME-TABLE

Name Of Staff: Prof. Geetanjali Aegade A.Y:-2021-22 SEM II WITH EFFECT FROM :

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
8:45 - 9:45		CN (GAA)				MC (GAA)			MC (GAA)		CN (GAA)				MC (GAA)
9:45 - 10:45									MC (GAA)		CN (GAA)				MC (GAA)
10:45 - 11:00	SHORT BREAK														
11:00- 12:00								MC (GAA)							
12:00- 01:00			MC (GAA)		CN (GAA)			MINI PROJE CT			MINI PROJE CT	MC (GAA)		MINI PROJE CT	
1:00 - 1:30	LUNCH BREAK														
1:30 - 2:30											CN (GAA)				
2:30-3:30		TNP				PS2		TNP	PS2		CN (GAA)	PS2		TNP	
3:30-4:30		TNP	PS2					TNP			CN (GAA)			TNP	

Time Table In-charge
Prof. Kalyani Kadam

Time table Coordinator
Prof. Kalyani Kadam

HOD
Prof. Prabhat Pallav

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Dr. Rahul Khandagale

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF__E&TC_ ENGINEERING

MASTER TIME-TABLE

Name Of Staff: Prof. Kalyani Kadam

A.Y.-2021-22 SEM II WITH EFFECT FROM :

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
8:45 - 9:45					PM (KAK)										
9:45 - 10:45	POCS (KAK)														
10:45 - 11:00	SHORT BREAK														
11:00- 12:00				POCS (KAK)						POCS (KAK)			DAL	PM (KAK)	
12:00- 01:00								MINI PROJECT		DAL	MINI PROJECT		DAL	MINI PROJECT	
1:00 - 1:30	LUNCH BREAK														
1:30 - 2:30							POCS (KAK)								
2:30-3:30							POCS (KAK)								
3:30-4:30							POCS (KAK)								

Time Table In-charge
Prof. Kalyani Kadam

Time table Coordinator
Prof. Kalyani Kadam

HOD
Prof. Prabhat Pallav

Principal
Dr. Rahul Khandagale

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF E&TC ENGINEERING

MASTER TIME-TABLE

Name Of Staff: Prof. Shubhangi Shelke

A.Y:-2021-22 SEM II WITH EFFECT FROM :

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
8:45 - 9:45				CS (SVS)											
9:45 - 10:45				ESD (SVS)						CS (SVS)					
10:45 - 11:00	SHORT BREAK														
11:00- 12:00	CS (SVS)						CS (SVS)						DAL		
12:00- 01:00	ESD (SVS)						CS (SVS)	MINI PROJECT		DAL	MINI PROJECT		DAL	MINI PROJECT	
1:00 - 1:30	LUNCH BREAK														
1:30 - 2:30				PBL						CS (SVS)			ESD (SVS)		
2:30-3:30				PBL						CS (SVS)			ESD (SVS)		
3:30-4:30				PBL						CS (SVS)			ESD (SVS)		

Time Table In-charge
Prof. Kalyani Kadam

Time table Coordinator
Prof. Kalyani Kadam

HOD
Prof. Prabhat Pallav

Principal
Dr. Rahul Khandagale

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE, PUNE

IT DEPT. Sem – I

ACADEMIC YEAR 2022-23

MASTER TIME TABLE

TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
9:00-10:00	COLD LAB(RK)	OS(CB)	ISR(JT)	COLD LAB(RK)	OS(CB)	ISR LAB(LP3)(JT)	COLD(RK)	OS(CB)	ISR LAB(LP3)(JT)	COLD(RK)	OS LAB(CB)	DA(JT)	COLD(RK)	OS LAB(CB)	[illegible]
10:00-11:00	OOPS(AB)	TOC(BG)	M.C(RK)	OOPS(AB)	TOC(BG)	M.C(RK)	OOPS(AB)	TOC(BG)	M.C(RK)	OOPS LAB(AB)	TOC(BG)	M.C(RK)	OOPS LAB(AB)	SEMINAR(BG)	PROJECT
11:00-11:30	SHORT BREAK														
11:30-12:30	DM(BG)	HCI(AB)	SEPM(JT)	DM(BG)	HCI(AB)	SEPM(JT)	DM(BG)	HCI(AB)	SEPM(JT)	DM(BG)	HCI(AB)	SEPM(JT)	SOFT SKILL(BG)	HCI LAB(AB)	PROJECT
12:30-13:30	LUNCH														
13:30-14:30	DSA(CB)	IOT(RK)	DL(AB)	DSA(CB)	IOT(RK)	DL(AB)	DSA(CB)	IOT(RK)	DL(AB)	DSA LAB(CB)	IOT(RK)	DL(AB)	DSA LAB(CB)	IOT(RK)	DL LAB(PK)…
14:30-15:30	BCN(JT)	ML(BG)	DEVOPS(CB)	BCN(JT)	ML(BG)	DEVOPS(CB)	BCN(JT)	ML(BG)	DEVOPS(CB)	BCN(JT)	ML LAB(BG)	DEVOPS(CB)	LIBRARY(JT)	ML LAB(BG)	PROJECT

TIME TABLE CO-ORDINATOR

HOD

PRINCIPAL

Prof. Chandramohan Sharma(CSm) | EM-II | SE | Prof. Avinash Tekale(AT)

CAYMET'S

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE,PUNE

Department of Information Technology

ACADEMIC YEAR 2021-22 SEM-II

MASTER TIME TABLE

DAY	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
TIME	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
08:45-09:45	EM III (AT)	CNS(XYZ)	CL-IX(JP)B1 / CL-X(CBS)B2	PAI(RK)	WAD (AB)	CL-IX(JP)B2/ CL-X(CBS)B1	SE(BY)	WAD (AB)	CL-IX(JP)B1/ EL III(RK)B2	SE(BY)	WAD (AB)	CL-IX(JP)B2/ EL III(RK)B1	DBMSL(XYZ)S2 / PBL(BG)S1	EL-II(CBS)	PROJECT WORK
09:45-10:45	DBMS(XYZ)	DS-BDA/(BG)		CG(JP)	DS-BDA/(BG)		DBMS(XYZ)	DS-BDA/(BG)		DBMS(XYZ)	EL-II(CBS)			LIBRARY	
10:45-11.00	SHORT BREAK														
11.00-12:00	PAI(RK)	CNSL(XYZ) T1/ INTERNSHIP T2	SMA(BY)	EM III (AT)	CNSL(XYZ) T2/ INTERNSHIP T1	SMA(BY)	PAI(RK)	CNSL(XYZ) T1/ LP-II/(AB)T2	SMA(BY)	PAI(RK)	LP-II/(AB)T3/ INTERNSHIPT2	SMA(BY)	SE(BY)	CNSL(XYZ) T2/ INTERNSHIPT3	PROJECT WORK
12:00-01:00	CG(JP)		INTERNET	CG(JP)	IOT(RK)	CG(JP)			UC(CBS)	EM III (AT)		DCS(JP)	CG(JP)		
01:00-01:30	LUNCH BREAK														
01:30-02:30	EM III (AT)	LIBRARY	IOT(RK)	SE(BY)	CNS(XYZ)	DCS(JP)	LIBRARY	CNS(XYZ)	IOT(RK)	CG(JP)	LIBRARY	IOT(RK)	EM III (AT)	DS-BDA/(BG)	PROJECT WORK
02:30-03:30	DBMSL(XYZ)S1/PBL(BG)S2	EL- II(CBS)	DCS(JP)	CGL(JP)S1/ PSDL(RK)S2	LP-II/(AB)	UC(CBS)	DBMSL(XYZ)S2/ PBL(BG)S1	EL- II(CBS)	DCS(JP)	DBMSL(XYZ)S1/ PBL(BG)S2	DS-BDAL/(AB)	DCS(JP)	CGL(JP)S2/ PSDL(RK)S1	DS-BDAL/(AB)	
03:30-04:30		WAD (AB)	UC(CBS)			LIBRARY		T & P	INTERNET			UC(CBS)			

Subjects Name	Class	Faculty Name
PBL, DS-BDA	TE, SE	Dr. Brijendra Gupta(BG)
PAI,PSDL,IOT,Project Work	SE, BE	Prof. Rashmi Kulkarni (RK)
DBMS, DBMSL, CNS, CNSL	TE, SE	[illegible]
EL-II, INTERNSHIP,IJC, CL -X	BE, TE	Prof. Chandrabhushan Sharma(CBS)

Subject Name	Class	Faculty Name
CG, CGL, DCS, CL-IX	SE, BE	Prof. Jyoti Pingalkar(JP)
SE, SMA	SE, BE	Prof. B. Yadav(BY)
WAD, CP-II, DS-BDA	TE	Prof. Ashwini Bhosale(AB)
EM-III	SE	Prof. Avinash Tekale(AT)

TT CO-ORDINATOR

HOD

PRINCIPAL

CAYMET'S
SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE,PUNE
Department Of Computer Engineering
ACADEMIC YEAR 2021-22 SEM-I
ONLINE LECTURES TIME TABLE
Class - SE

TIME	Mon	Tue	Wed	Thurs	Fri
10:00 to 11:00 PM	DM (RP)	DM (RP)	DM (RP)	DM (RP)	DEL & D (MD)
11:00 to 12:00 PM	CG (CPS)	OOP (SY)	OOP (SY)	OOP (SY)	OOP (SY)
1:00 to 2:00 PM	FDS (KJ)	FDS (KJ)	FDS (KJ)	DEL & D (MD)	CG (CPS)
2:00 to 3:00 PM	DEL & D (MD)	DEL & D (MD)	CG (CPS)	CG (CPS)	FDS (KJ)

Subject Name	Faculty Name
Discrete Mathematics(DM)	Prof.Rupali Panpaliya (RP)
Fundamental of Data Structure(FDS)	Prof. Kavita Jadhav(KJ)
Object Oriented Programming(OOP)	Prof.Sunil Yadav(SY)
Computer Graphics(CG)	Prof.Chetana Pradip Shravage(CPS)
Digital Electronics & Logic Design (DEL & D)	Prof.Manisha Damk(MD)

for
Prof. Chetana Shravage
TT CO-ORDINATOR

Prof. Sunil Yadav
HOD

Prof. U.V.Shinde
PRINCIPAL

CAYMET'S
SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE,PUNE
Department Of Computer Engineering
ACADEMIC YEAR 2021-22 SEM-I
ONLINE LECTURES TIME TABLE
Class - TE

TIME	Mon	Tue	Wed	Thurs	Fri
10:00 to 11:00 PM	DBMS (CPS)	DBMS (CPS)	DBMS (CPS)	CN & S (AT)	CN & S (AT)
11:00 to 12:00 PM	CN & S (AT)	SPOS (KJ)	CN & S (AT)	SPOS (KJ)	IOT & ES (AB)
1:00 to 2:00 PM	SPOS (KJ)	IOT & ES (AB)	IOT & ES (AB)	IOT & ES (AB)	SPOS (KJ)
2:00 to 3:00 PM	TOC (SM)	TOC (SM)	TOC (SM)	TOC (SM)	DBMS (CPS)

Subject Name	Faculty Name
Database Management System(DBMS)	Prof.Chetana Shravage (CPS)
Theory of Computation(TOC)	Prof. Seema Mahalunglkar(SM)
System Programming & Operating System(SPOS)	Prof.Kavita Jadhav (KJ)
Computer Network & Security(CN & S)	Prof.Aparna Thakre(AT)
Elective-I Internet of Things & Embedded System (IOT & ES)	Prof.A.Bagwan(AB)

for

Prof. Chetana Shravage
TT CO-ORDINATOR

Prof. Sunil Yadav
HOD

Prof. [illegible] Shinde
PRINCIPAL

CAYMET'S
SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE,PUNE
Department Of Computer Engineering
ACADEMIC YEAR 2021-22 SEM-I
ONLINE LECTURES TIME TABLE
Class - BE

TIME	Mon	Tue	Wed	Thurs	Fri
10:00 to 11:00 PM	AI & R (AB)	AI & R (AB)	AI & R (AB)	AI & R (AB)	E-I DMW (SM)
11:00 to 12:00 PM	E-I DMW (SM)	E-I DMW (SM)	E-I DMW (SM)	DA (SS)	DA (SS)
1:00 to 2:00 PM	DA (SS)	DA (SS)	E-II STQA (SY)	E-II STQA (SY)	E-II STQA (SY)
2:00 to 3:00 PM	HPC (SS)	E-II STQA (SY)	HPC (SS)	HPC (SS)	HPC (SS)

Subject Name	Faculty Name
High Performance Computing(HPC)	Prof.Sushma Shinde (SS)
Artificial Intelligence & Robotics(AI & R)	Prof. A. A.Bagwan(AB)
Data Analytics(DA)	Prof.Sushma Shinde (SS)
Elective-I Data Mining & Warehousing(DMW)	Prof.Seema Mahulangkar(SM)
Elective-II Software Testing & Quality Assurance (STQA)	Prof.Sunil Yadav(SY)

for
Prof. Chetana Shravage
TT CO-ORDINATOR

Prof. Sunil Yadav
HOD

Prof. P.V.Shinde
PRINCIPAL

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF COMPUTER ENGINEERING

MASTER TIME-TABLE Sec - A

SEM II

A.Y.-2021-22

WITH EFFECT FROM : 21/03/22

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
8:45 - 9:45	DSA/(PK)	AI/(AC)	ELE-III/(AB)	MP/ (AT)	DSBDA/ (RP)	ML/(SY)	PPL/(MD)	AI/(AC)	ML/(SY)	SE/(AB)	DSBDA/ (RP)	ICS/(AC)	PPL/ (MD)	AI/(AC)	ELE-IV/(SJ)
9:45 - 10:45	MP/(AT)	SMA/ (MD)	ML/(SY)	SE/(AB)	AI/(AC)	ELE-IV/ (SJ)	DSA/(PK)	DSBDA/ (RP)	ELE-III/(AB)	MP/(AT)		ML/(SY)	SE/(AB)	DSBDA/ (RP)	ML/(SY)
10:45 - 11:00	SHORT BREAK														
11:00- 12:00	M-III/ (NK)	DSBDA/(RP)	ICS/(AC)	DSA/ (PK)	SMA/ (MD)	ELE-III/(AB)	M-III/(NK)	WT/(SS)	ELE-IV /(SJ)	PPL/(MD)	AI/(AC)	ELE-III/(AB)	M-III/(NK)	SMA/ (MD)	ICS/(AC)
12:00- 01:00	PPL/(MD)	WT/(SS)	ELE-IV /(SJ)	M-III /(NK)	WT/(SS)	ICS/(AC)	MP/(AT)	SMA/ (MD)	ICS/(AC)	M-III /(NK)	WT/(SS)	ELE-IV /(SJ)	DSA/ (PK)	WT/(SS)	ELE-III /(AB)
1:00 - 1:30	LUNCH BREAK														
1:30 - 2:30	SE/(AB)	INTERNSHIP	Project Work	PPL/ (MD)	INTERNSHIP	Project Work	SE/(AB)	INTERNSHIP	Project Work	DSA/(PK)	SMA/ (MD)	Project Work	MP/(AT)	INTERNSHIP	Project Work
2:30-3:30	LH	T&P SESSION		LH			CODE OF CUNDUCT	T&P SESSION		LH	INTERNSHIP		LH	T&P SESSION	
3:30-4:30	Mini Project		LH	Mini Project	Mini Project	LH	LH		LH	Mini Project		LH	Mini Project		LH

Time Table In-charge
Dr. Aniket Deshpande

Time table Coordinator
Prof.Rupali Panpaliya

HOD
Prof. Sunil Yadav

Principal
Dr. Rahul Khandagale

CLASS	NAME OF CLASS COORDINATOR
SE	Prof. Aparna Thakare
TE	Prof. Archana Chaliv
BE	Prof. Sushma Shinde

CLASS	ROOM NO
SE	C-23
TE	C-24
BE	C-20

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF COMPUTER ENGINEERING

MASTER TIME-TABLE Sec - B

SEM II

A.Y.-2021-22

WITH EFFECT FROM : 21/03/22

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
8:45 - 9:45	Code of conduct	WT/(SS)	ML/(SY)	PPL/(MD)	INTERNSHIP	ELE-IV/ (SJ)	LH	WT/(SS)	ELE-III/(RP)	DSA/(PK)	INTERNSHIP	ICS/(AT)	SE/(AB)	DSBDA/ (RP)	ICS/(AT)
9:45 - 10:45	SE/(AB)	DSBDA/(RP)	ELE-IV/(SJ)	DSA/(PK)	WT/(SS)	ELE-III/(RP)	MP/ (AT)	SMA/(SJ)	ML/(SY)	PPL/(MD)	WT/(SS)	ELE-IV/(SJ)	DSA/(PK)	AI/(AC)	ELE-IV/(SJ)
10:45 - 11:00	SHORT BREAK														
11:00- 12:00	M-III	SMA/(SJ)	ICS/(AT)	MP/(AT)	DSBDA/ (RP)	ML/(SY)	M-III	DSBDA/ (RP)	ICS/(AT)	MP/(AT)	SMA/(SJ)	ELE-III /(RP)	M-III	WT/(SS)	ML/(SY)
12:00- 01:00	MP/(AT)	INTERNSHIP	ELE-III/(RP)	M-III	SMA/(SJ)	ICS/(AT)	DSA/ (PK)		ELE-IV/(SJ)	M-III	DSBDA/ (RP)	ML/(SY)	MP/(AT)	SMA/(SJ)	ELE-III /(RP)
1:00 - 1:30	LUNCH BREAK														
1:30 - 2:30	PPL/(MD)	AI/(AC)	Project Work	SE/(AB)	AI/(AC)	Project Work	PPL/(MD)	AI/(AC)	Project Work	SE/(AB)	AI/(AC)	Project Work	PPL/(MD)	INTERNSHIP	Project Work
2:30-3:30	DSA/(PK)	T&P SESSION		LH	Class Work		SE/(AB)	T&P SESSION		LH	INTERNSHIP		LH	T&P SESSION	
3:30-4:30	Mini Project		LH	Mini Project	LH	LH	LH		LH	Mini Project	Mini Project	LH	Mini Project		LH

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CLASS	ROOM NO
SE	B-10
TE	B-12
BE	B-11

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF COMPUTER ENGINEERING

MASTER TIME-TABLE Sec - B

SEM B

A.Y:-2021-22

WITH EFFECT FROM : 21/03/22

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
8:45 - 9:45	Code of conduct	WT/(SS)	ML/(SY)	PPL/(MD)	INTERNSHIP	ELE-IV/ (SJ)	LH	WT/(SS)	ELE-III/(RP)	DSA/(PK)	INTERNSHIP	ICS/(AT)	SE/(AB)	DSBDA/ (RP)	ICS/(AT)
9:45 - 10:45	SE/(AB)	DSBDA/(RP)	ELE-IV/(SJ)	DSA/(PK)	WT/(SS)	ELE-III/(RP)	MP/ (AT)	SMA/(SJ)	ML/(SY)	PPL/(MD)	WT/(SS)	ELE-IV/(SJ)	DSA/(PK)	AI/(AC)	ELE-IV/(SJ)
10:45 - 11:00	SHORT BREAK														
11:00- 12:00	M-III	SMA/(SJ)	ICS/(AT)	MP/(AT)	DSBDA/ (RP)	ML/(SY)	M-III	DSBDA/ (RP)	ICS/(AT)	MP/(AT)	SMA/(SJ)	ELE-III /(RP)	M-III	WT/(SS)	ML/(SY)
12:00- 01:00	MP/(AT)	INTERNSHIP	ELE-III/(RP)	M-III	SMA/(SJ)	ICS/(AT)	DSA/ (PK)		ELE-IV/(SJ)	M-III	DSBDA/ (RP)	ML/(SY)	MP/(AT)	SMA/(SJ)	ELE-III /(RP)
1:00 - 1:30	LUNCH BREAK														
1:30 - 2:30	PPL/(MD)	AI/(AC)	Project Work	SE/(AB)	AI/(AC)	Project Work	PPL/(MD)	AI/(AC)	Project Work	SE/(AB)	AI/(AC)	Project Work	PPL/(MD)	INTERNSHIP	Project Work
2:30-3:30	DSA/(PK)	T&P SESSION		LH	Class Work		SE/(AB)	T&P SESSION		LH	INTERNSHIP		LH	T&P SESSION	
3:30-4:30	Mini Project		LH	Mini Project	LH	LH	LH		LH	Mini Project	Mini Project	LH	Mini Project		LH

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TE	B-12
BE	B-11

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SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109

DEPARTMENT OF CIVIL ENGINEERING

MASTER TIME-TABLE (SEM I) - YEAR:-2021-22

DAY TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
08:30-09:25	M-III	HWRE	E III	EG	CM	TRE	BT&AP	CM	E-IV	BT&AP	HWRE	ACI (B1)	AC	WSE	E-IV
09:25-10:20	EG	CM	E-IV	MOS	HWRE	E-III	EG	DSS	AC I (B2)	MOS	DSS	TRE	M-III	DSS	AC I (B2)
10:20-10:50	R			E			C			E			S		S
10:50-11:45	FM	DSS	FE	FM	DSS	E-IV	M-III	SEMINAR T1	E-III	EG	CM	E III	S1 &S2-BTAP	ESD (PR)	Project
11:45-12:40	MOS	EE & FM	TRE	BT&AP	WSE		MOS	WSE	TRE	AUDIT.C	SEMINAR (T2)				
12:40-01:30	R			E			C			E			S		S
01:30-02:25	BT& AP	WSE	Application to Python	M-III	EE & FM	FE	M-III (TUT)	EE & FM	FE	FM	EE & FM	FE	FM	AUD-I	Application to Python
02:25-03:20	MOS (S1) FM - (S2)	T1-DSS T2-HWRE	B1-Python B2-TRE	EG-(S1) MOS (S2)	T1-CM T2-WSS	Project	EG-(S2) BT&AP-(S1)	T1-WSS T2-CM -	E- III(B1) E-IV (B2)	BT&AP - (S2) FM (S1)	T1- HWRE T2-DSS	E- III(B2) E-IV (B1	S1 AND S2 - MOS	T1&T2 - DSS	B2-python B1-TRE
3:20-04:15															

Time Table coordinator

HOD

Principal

29

CAYMET's
SIDDHANT COLLEGE OF ENGINEERING, SUDUMBARE PUNE-412109
DEPARTMENT OF CIVIL ENGINEERING
MASTER TIME-TABLESEM -II YEAR:-2021-22
SEM-II

DAY / TIME	MONDAY			TUESDAY			WEDNESDAY			THURSDAY			FRIDAY		
	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE	SE	TE	BE
8:45-9:45	CT	RS & GIS	CM	SA	SWM (EL II)	DHS	SUR	WWE	QSCT	SA	DR CC	DHS	PM	DRCC	
9:45 10:45	SUR	SWM (EL II)	QSCT	CT	WWE	APC	CT	RS & GIS	CM	GTE	AC	QSCT	SA	SWM (EL II)	
10:45 11:00				SHORT BREAK											
:00 :00	GTET (S1)	DRCC	PROJECT	SURVEY (S1) GTE (S2)	DRCC (T1) RS & GIS (T2	PROJECT	PM	DRCC (T2) RS & GIS(T1)	QSCT (B1) APC(B2)	PBL (ASD)	WWE PR (T1)	QSCT (B2) APC(B1	SUR	WWE (PR) (T2)	PROJECT
2:00 1:00	SURVEY (S2)	WWE					GTE						GTE		
1:00 1.30				LUNCH BREAK											
1:30-2:30	TU	SWM	APC	PM	LH	CM	LH	RS & GIS	LH	LH	LH	LH	LH	LH	LH
2:30-3:30	PBL (ASD)	T&P	PROJECT (STUDENT WORK TIME)	CT (S2) SURVEY (S1)	DRCC (T1 SWM (EL II)(T2)	DHS (B1) CM(B2)	PBL (BBD)	T&P	DHS (B2) CM(B1)	SURVEY (S2) CT (S1)	DRCC (T2 SWM (EL II)(T1)	PROJECT (STUDENT WORK TIME)	PBL (BBD)	T&P	PROJECT (STUDENT WORK TIME)
3:30-4:30															

T.T Coordinator

HOD

Principal

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING

Sudumbare, Pune – 412109

CERTIFICATE OF COMPLETION

Subject Electronic Circuits

This is to certify that Mr/~~Mrs~~ Abhijeet Arvind Naik

Of E & TC (SE) Roll No.

University Exam No. has satisfaction only complete the Required number of practical/ Term Work as laid down by university.

Date:- 29/12/2021

29/12/21

Subject Teacher

Head Of The E&TC Dept.
Siddhant College of Engineering
Sudumbare, Maval, Pune- 412109

Principal
Siddhant College of Engineering
Sudumbare, Pune - 412 109

CAYMET's

SIDDHANT COLLEGE OF ENGINEERING

Sudumbare, Pune – 412109

Department of E&TC Engineering

A.Y. – 2021-22

Subject - Electronic Circuits

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3	Assignment 3	15	19	
4	Assignment 4	21	27	
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6	Assignment 6	37	43	
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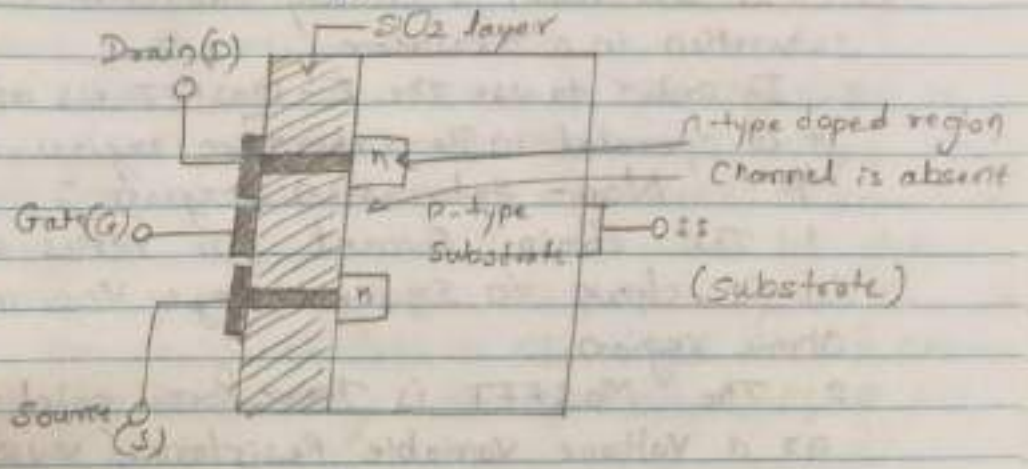
8				
9				
10				

Gaikwad

Subject Teacher

Topic : Electronic Circuits - Unit I

1) Draw the constructional diagram of N channel E-MOSFET & Give drain and transfer characteristics for the same with necessary parameters.



Drain characteristics :

1. Drain characteristics is a plot of drain current I_D (on Y-axis) versus drain to source voltage V_{DS} (on x-axis) at different values of gate to source voltage V_{GS}.
2. The drain characteristics has been divided into three regions i.e. cutoff, saturation and ohmic region.

* Cutoff region :

1. It corresponds to drain current $I_D = 0$
2. At a certain voltage called $V_{GS(off)}$ the drain current reduced to zero.
3. Hence the cutoff region corresponds to $I_D = 0$ & $V_{GS} \leq V_{TN}$
4. The E-MOSFET operates as an open circuited switch in this region.

1. Saturation region is that portion of the characteristics

Where I_D remains fairly constant & does not change with changes in V_{DS}.

2. The saturation is entirely different than the saturation in a transistor.

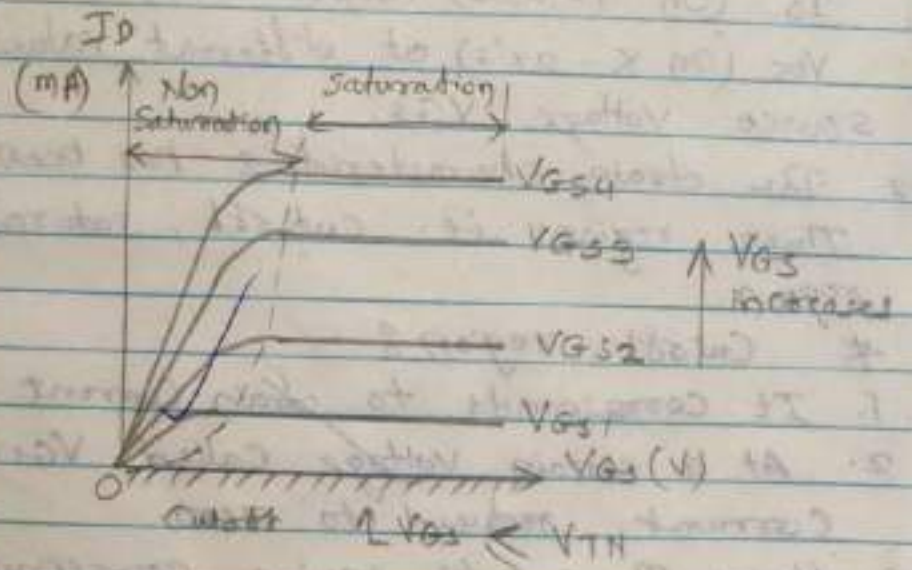
3. In order to use the E-MOSFET as an amplifier it is operated in the saturation region.

* Non-saturation region :

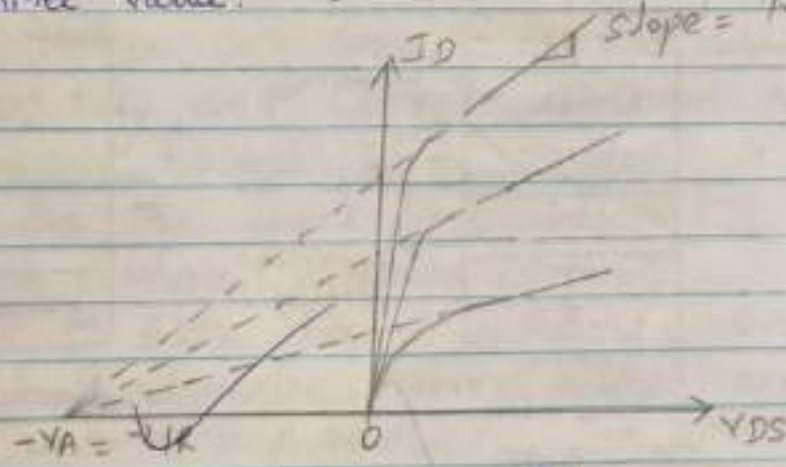
1. The drain current I_D varies with variation in the drain to source voltage V_{DS}, in the ohmic region.

2. The MOSFET is therefore said to be operating as a voltage variable resistance (VVR) in the ohmic region.

3. It is equivalent to a closed switch in this region



2. Explain the non ideal current voltage characteristics
i. Finite o/p resistance ii channel length modulation
iii. Body effect iv subthreshold conduction
v. Breakdown effect vi Temperature effect
i. Finite o/p resistance
1. ~~let~~ lets us assume that the MOSFET is independant of the drain to source voltage V_{DS}.
2. The I-V characteristics of MOSFET is shown in diagram. The curves can be extended by dotted lines till they intersect the x-axis at point $V_{DS} = -V_A$
4. The o/p resistance (r_o) is the slope of V-I characteristics. It should be ideally ∞ but practically it has some finite value.

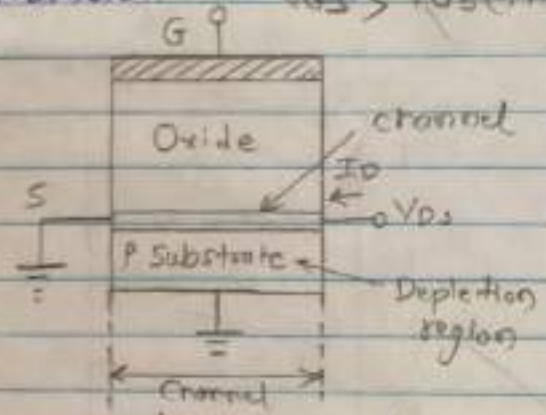


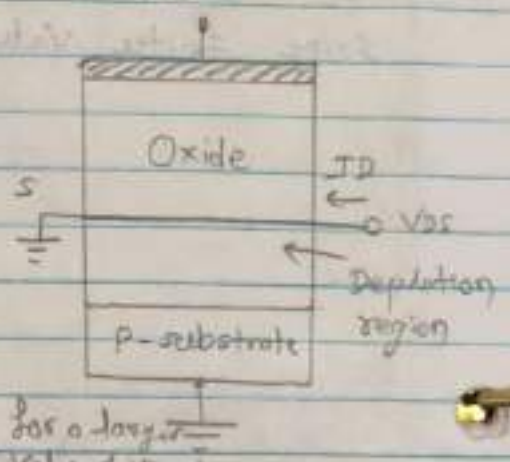
5. The voltage V_A is usually defined as a positive quantity & it is similar to the early voltage of ~~the~~ bipolar transistor.
6. The I_D versus V_{DS} characteristics can be mathematically expressed as,

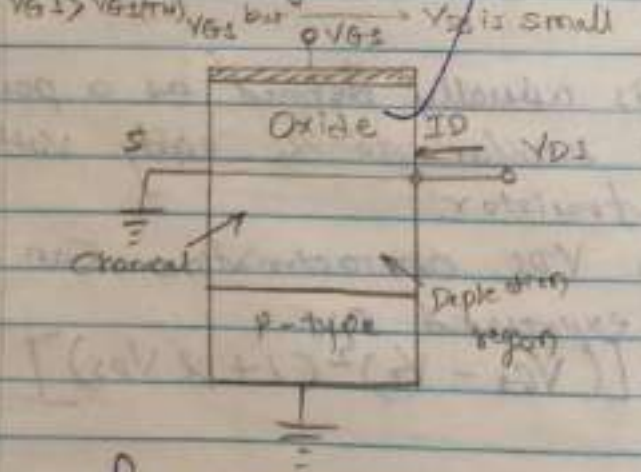
$$I_D = k[(V_{GS} - V_T)^2 (1 + \lambda V_{DS})]$$

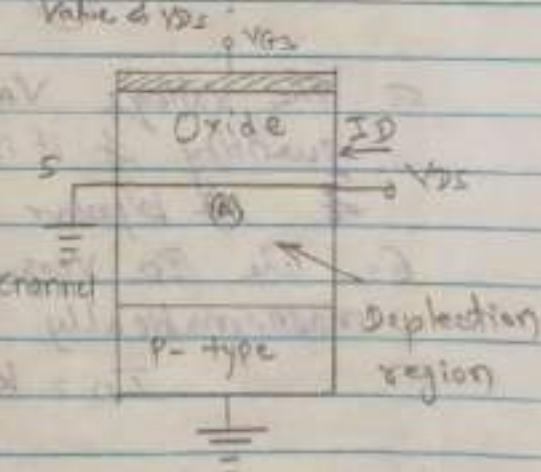
1. Channel length modulation

1. The finite value of r_o is due to a phenomenon called channel length modulation.
2. The voltage V_A is usually defined as a positive quantity & it is similar to the early voltage of the bipolar transistor.
3. The I_D versus V_{DS} characteristics can be expressed as $I_D = k[(V_{GS} - V_T)^2(1 + \lambda V_{DS})]$
4. In this expression, λ is a positive quantity & called as the channel length modulation parameter.









for $V_{DS} = V_{DS(sat)}$ $V_{DS} > V_{DS(sat)}$

5. For $V_{DS} > V_{DS(sat)}$, the actual point in the channel at which the inversion charge goes to zero, moves away from the drain terminal.

6. Therefore the effective channel length decreased This phenomenon is called as channel length modulation.

iii Body effect

1. The operation of a MOSFET has been explained by assuming that the body or substrate has been connected to source.
2. When the 2 MOSFETs are conducting, the drain to source voltage will have a non zero value.
3. When body and source are connected together, the threshold voltage V_T is constant.
4. Therefore the source terminal of M2 will not be at the substrate potential (ground)
5. Thus M1 & M2 are at different potentials
6. Therefore a zero/or reverse voltage appears across the source to body junction.
7. And change in the source body junction voltage will change the threshold voltage. This is called Body effect.

iv Subthreshold conduction

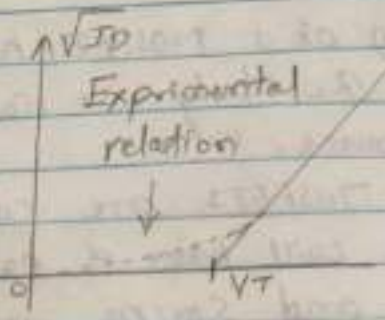
1. If an n-channel MOSFET is biased to operate in saturation region, then the ideal current voltage relationship is expressed as,

$$I_D = k (V_{GS} - V_T)^2$$

2. Taking Square root of both sides we get

$$\sqrt{I_D} = \sqrt{k} (V_{GS} - V_T)$$
$$= \sqrt{k} V_{GS} - \sqrt{k} V_T$$

3. This expression represents a straight line. That means $\sqrt{I_D}$ has a linear relationship with V_{GS}.



4. But practically we don't get this linear relationship The practical characteristics is nonlinear as shown by dotted characteristics.
5. The dotted characteristics also shows that the drain current is non zero for $V_{GS} < V_T$, where theoritically it should be zero
6. This current is called as sub threshold current.

V. Breakdown Effects

1. Avalanche breakdown: If drain (n+) to substrate (P), P-n junction is subjected to a large reverse voltage by increasing V_{DD} then this junction may breakdown due to avalanche breakdown.

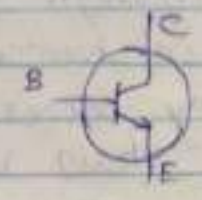
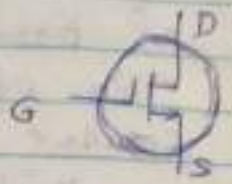
2 ~~Punk~~ Punch through breakdown: Another type of breakdown mechanism is punch through effect This effect may occour if size of device becomes Smaller. As The drain Voltage is increased beyond a particular Value, The depletion region around The drain will extend completly through The channel to Source terminal. This is called as punch Through.

3. Near - avalanche or snapback breakdown: This is The third breakdown mechnism. It takes place due to second order effects within MOSFET. At The due of MOSFET reduces, we may notice a ~~parasi~~ Parasitic BJT acting with increase in drain Voltage.

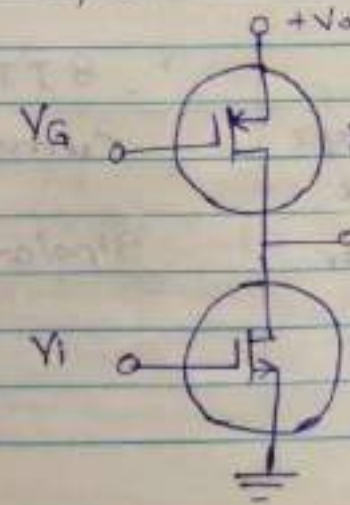
4. Breakdown due to static charge: Due to high input impedance of The MOSFET, a very small static charge accumulated on The gate can exceed breakdown can be avoided if we don't allows The accumulation of charge to take place on The gate capacitance.

3. Differentiate between BJT & MOSFET

→ Parameter	BJT	MOSFET
1. Current / Voltage Controlled device	Current	Voltage
2. unipolar / bipolar device	Bipolar	Unipolar

3. Symbol	 	 
4. Size	Small	Very small.
5. Controlling terminal	Base	Gate
6. Transfer Charac	Linear	Nonlinear
7. Thermal runaway	Can take place	Does not take place
8. Isolation of Controlling terminal from device structure	Base is not Isolated	Gate is isolated
9. I/p resistance	low/moderate	Very high.
10. Noise produced	High	Very low.
switching speed	low	High.

4. Explain the principle of BiCMos technology



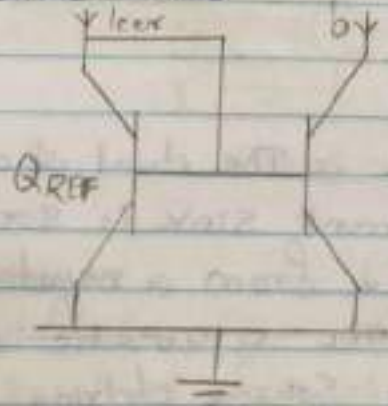
1. A p-channel enhancement mode MOSFET (M_1) can be used as load for an n-channel enhancement mode MOSFET M_2 to form a Complementary MOS (CMOS) inverter.
2. The term Complementary suggests that both n- channel & p-channel MOSFET's are used in the same circuit.
3. The CMOS tech is very popular technology & it is used in both analog & digital electronic ckts.
4. Figure shows a CMOS inverter in which the PMOS acts as a load & NMOS device acts as the driver

Gurjeet

(1) What is Current mirror and also state the advantages & Calculate Current mirror

→ Current mirror - is explicitly used in VLSL design in order to design a constant current source which is required in some or the other parts in VLSI Circuits

This can be easily achived by forming a circuit like - this



Here, transistor Qref is fixed based and the collector terminal is connected to positive supply. Hence the current though that transistor remains the same

Advantages Cascode Current Mirror

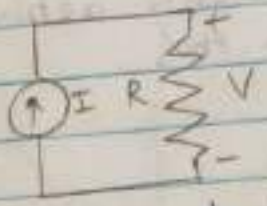
(1) Cascade current mirror elimination the channel length modulation effect by keeping $V_{ds1} = V_{ds2}$ constant in the ratio:

$$I_{out} = I_{ref} \frac{(W/L)(1+\lambda V_{ds})}{(W/L)(1+\lambda V_{ds})}$$

(2) Improves output resistance

(2) state methods of performance improvement of current source / sink and explain any one of them.

→ Current Source is an electronic Circuit That delivers or absorbs an electric current which independent of The voltage across it



A Current Source is The dual of a voltage source. The term Current sink is sometimes used The term source Fed from a negative voltage supply figure shows The schematic symbol for an ideal Current Source driving a resistance load. There are two type an independence Current Source (or sink) delivers a constant Current a dependent Current source delivers a Current which is propr^n to some other voltage or Current Circuit.

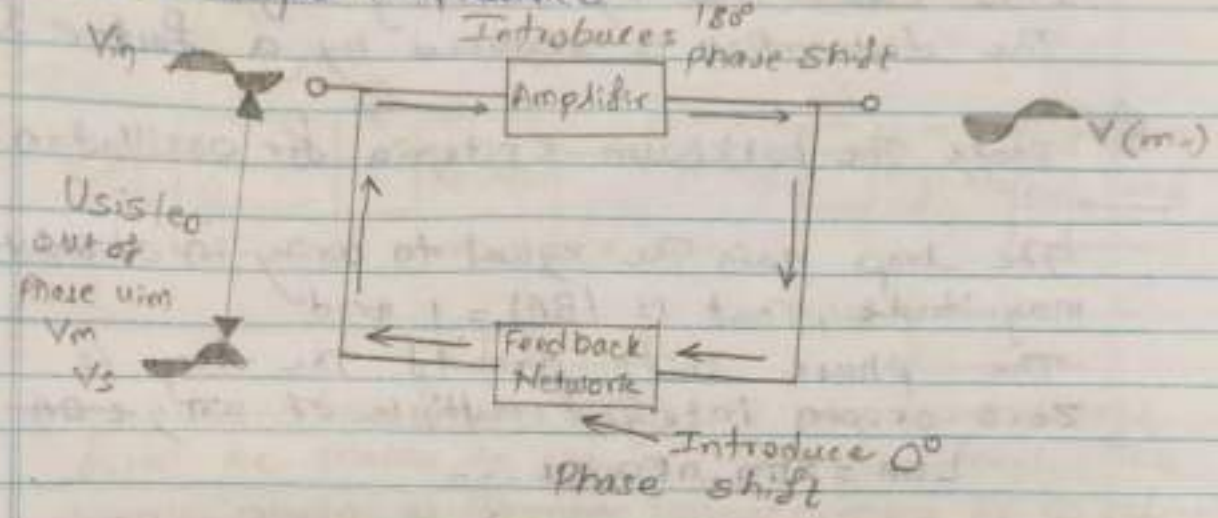
(3) what is The effect of negative feed back on gain, stability distortion and Bandwidth

→ Negative Feedback —

In negative feedback, The feed back energy (voltage or Current), is out of phase with The input signal and thus opposes it.

Negative feedback reduces gain of The amplifier, It also reduce distortion, Noise and instability.

This feedback increase bandwidth and improved input and output impedance



Gain stability –

An important advantage of negative V feedback is that the resultant gain of the amplifier can be made independent of transister parameters or the supply voltage variations

$$AF = A/(1+AB)$$

Distrordion –

A power amplifire will have non-linear distrordion because of large signal variation The negative feedback reduce the nonlinear distrordion It can be provide mathematically that

$$Dt = D/(1+AB)$$

where, D = distrordion in amplifire without feedback

Dt = distrordion in amplifire with negative

feedback
It is clear that by applying negative feedback The distortion is reduced by a factor (1+AB)

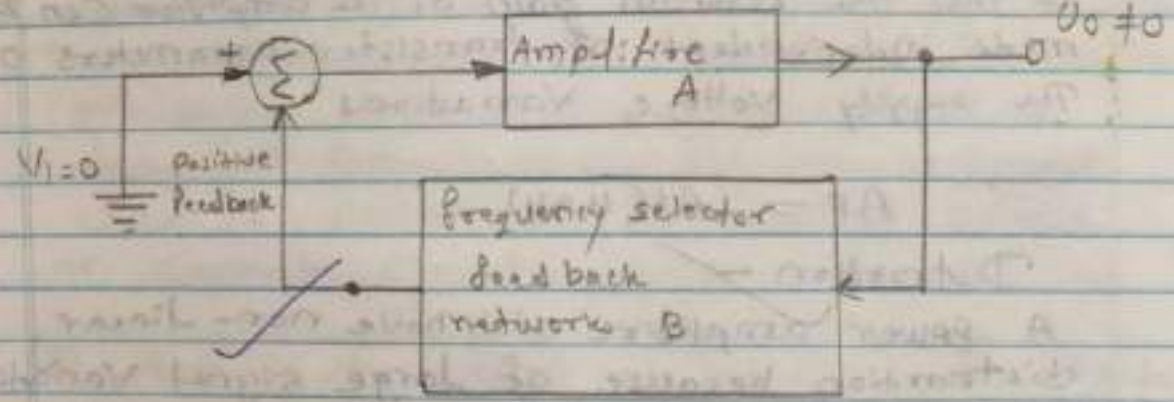
(4) State The barkhaun criteria for oscillation of ckt.

→

The loop gain The equal to unity in absolute magnitude, That is |BA| = 1 and
The phase shift around The loop is zero or an integer multiple of 2π; ~~∠BA~~

∠BA = 2πn, n=0, 1, 2 - - -

The product BA is called as The 'loop gain"

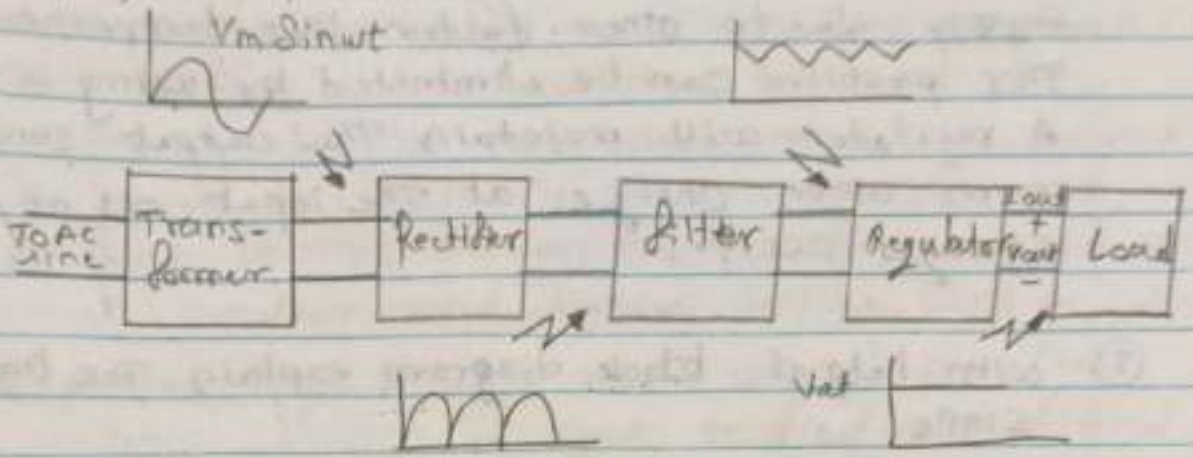


Barkhausen's Criteria of oscillation

Conclude.

Unit III

(1) Draw the block diagram of regulated Dc power supply. explain the function of each block in it



1) stepdown transformer:- It will stepdown voltage from Ac mains to required voltage level. The turn's ratio of ~~Transformer~~ transformers is so adjusted such as required voltage value can be optained. The O/P of transformer is given to rectifier Circuit

2) Rectifier :- is an electronics circuit consisting of diode which carries out the rectification process. The input to rectifies is an ac where it output is unidirectional pulsating dc. Usually a full wave rectifier bridge rectifies is used to rectify both half cycle of the ac supply.

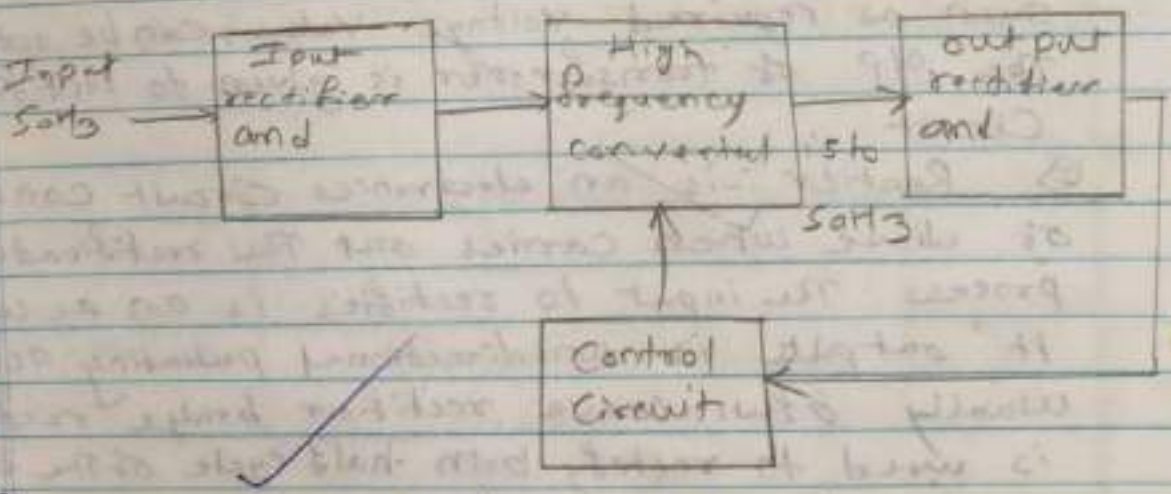
3) filter :- The rectified voltage from rectifier is a pulsating dc voltage having very high ripple content hence filter is used.

4) Regulator:- This the last block in regulated Dc power supply the output voltage as current will change as fluctuate when there in change in the input from ac mains as the change in

Load current at the output of the regulated power supply due to other factor like temperature change This problem can be eliminated by using a regulator A regulator will maintain the output constant even when change at the input as any other changes occur.

(2) with help of block diagram explain the basic SMPS.

→ The working of SMPS can be understand by following figure.

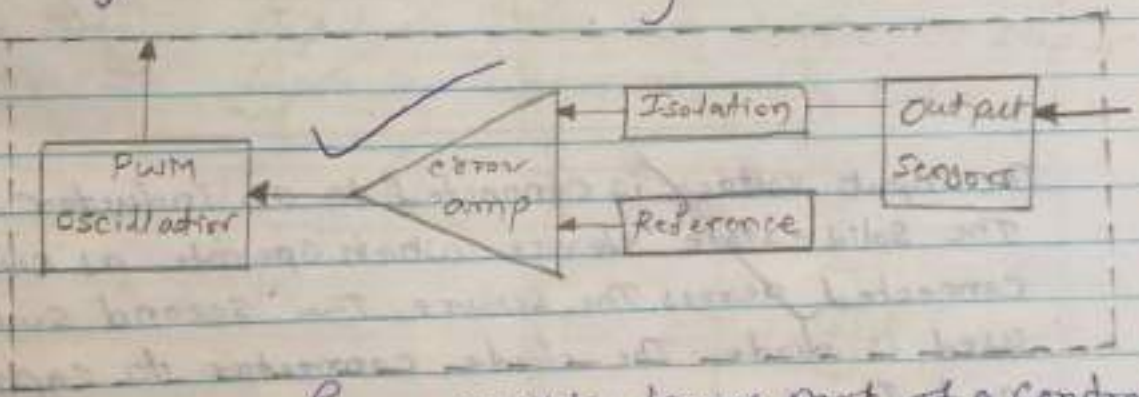


(1) Input stage :- The AC input signal 50Hz is given directly to rectifier and filter circuit combination without using Actransformer This output have many variation and the capacitance value of the capacitor should be higher to handle the up fluctuation This unregulated Dc is given to Control Switching section of SMPS.

2) Switching Section :- A fast switch devices such as power transistor as MOSFET is employed in this section which switched on and off according to the variations and this output is given to primary of the transformer present in this section the transformer used are much smaller and lighter unlike used in SMPS.

3) output stage :- The output signal form the switching section is again rectified and filtered to get the required DC voltage which is given to the control circuit which feedback circuit the final output is obtained after considering the feedback signal.

4) control unit :- This is feedback circuit has many section the following figure shown below.

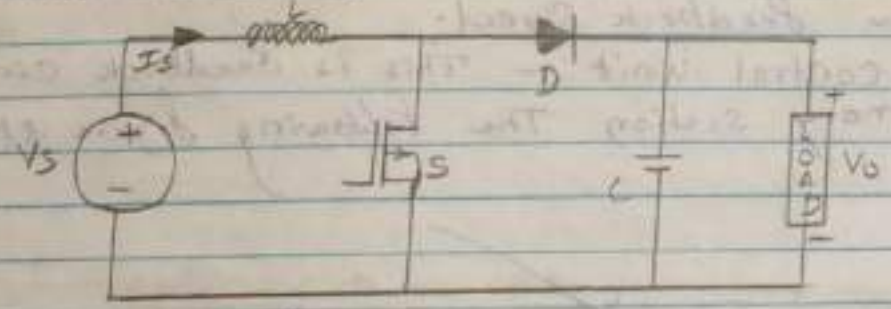


The above figure explain inner part of a control unit. The output sensor the signal and joins it to the control unit. The signal is isolated from the other section so that sudden spikes should not affect the circuitary A reference voltage is given as one input along with signal to error amplifier which is comparator that compares

This signal with required signal level by controlling the chopping frequency The final voltage level is maintained This is controlled by comparing input given to error amplifier, whose o/p help to decide whether to increase as oscillator Produces a standard PWM wave fixed frequency.

3) Describe the boost convertor & buck boost convertor

→ Boost Convertor:- DC-DC converter are also known as chopper A stepup chopper is called as boost converter. It increase the input DC voltage to specified DC output voltage. A typical boost convertor is shown below

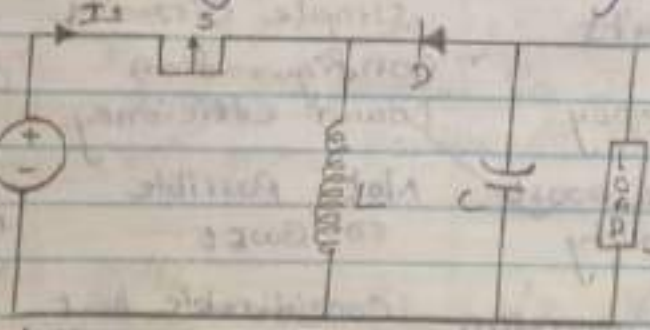


The input voltage is connected to an inductor The Solid-state device which operate as switch is connected across the source The second switch used is diode. The diode connector to capacitor and the load and two are connected in parallel.

The inductor connected to input source load ~~Constat~~ constant current and thus the Boost convertor is seen as constant current input source. The controlled switch is turned on/off by using P wm. PWM can be time based or frequency based. Boost convertor has two mode of operation.

1st mode switch is operated and current through inductor is made continous. In this energy is stored 2nd mode switch is off and diode is on. In this mode, energy stored in inductor is released This helps to maintain flow of current in some direction.

2) Buck boost Convertor: The buck boost convertor is type of Dc-Dc converter (also known as chopper) that has an output voltage magnitude either greater than or less than the input voltage. magnitude it is equivalent to flyback convertor using a single inductor instead of transformer two different topologies are called as buck boost convertor Dc-Dc convertor also known as chopper Here we have a look at buck Boost Convertor which operates as Dc-Dc stepdown Convertor as DC-Dc stepup convertor depending upon the duty cycle.



The input voltage is connected to solid state device The second switch used is a diode. The diode is connected in reverse direction of power flow from source to a Capacitor. and Load are connected in parallel. The controlled switch is to on and off using PWM. PWM can be time base as frequency

1st mode · switch is on and Diode off. Current flow to Inductor and back to dc input source Indicator stage charge during this when switch is off polarity Inductor reverse and current through load Through diode and back to Inductor
2nd Mode · switch off and diode ON.

4) comparison between linear and switching mode regulator.

	Linear Regulator	Switching Regulator.
1) Components used	Linear components such as resistor Load to regulator	Switch regulator switch elements to transform the incoming supply in phased voltage. MOSFETs are used.
2) Circuits	Simple Circuits configuration	Complex Circuit used
3) efficiency	Lower efficiency	High efficiency.
4) Buck boost Possibility	Not Possible to Boost	Buck / boost/ Negative voltage operation Positive
5) Heat generation	Considerable heat generation	Low heat generation
6) Noise levels	Low noise	Increase noise.

Argued.

ASSIGNMENT NO-4

Q.1. Analyse the dual input balanced output differential amplifier to obtain the following:
1) Differential gain 2) common mode gain
3) O/P resistance 4) I/P resistance.

Ans:i) To perform the ac analysis of dual input balanced output differential amplifier, following are the steps-
Step 1 = set the dc voltages $+V_{CC}$ & $-V_{EE}$ to zero i.e. short them to ground
Step 2 - Replace the transistors Q_1 & Q_2 with their small signal T- equivalent models.

ii) fig(a) shows the resulting ac equivalent circuit of the dual - input balanced - output differential amplifier.

iii) As $I_{E_1} = I_{E_2}$, we can write that $r_{e_1} = r_{e_2}$ Hence A ac emitter resistance of transistor Q1 & Q2 are equal to re i.e. $r_{e_1} = r_{e_2} = r_e$

iv) The voltage across each collector resistor Rc is out of phase by 180° wrt. V_{S1} & V_{S2}. Note that Polarity assigned to O/P voltage V_o. It indicator voltage at collector C_2 is more positive to voltage at C_1

1) Differential gain —
Output voltage $V_o = \frac{R_c}{r_e}(V_{S1} - V_{S2})$

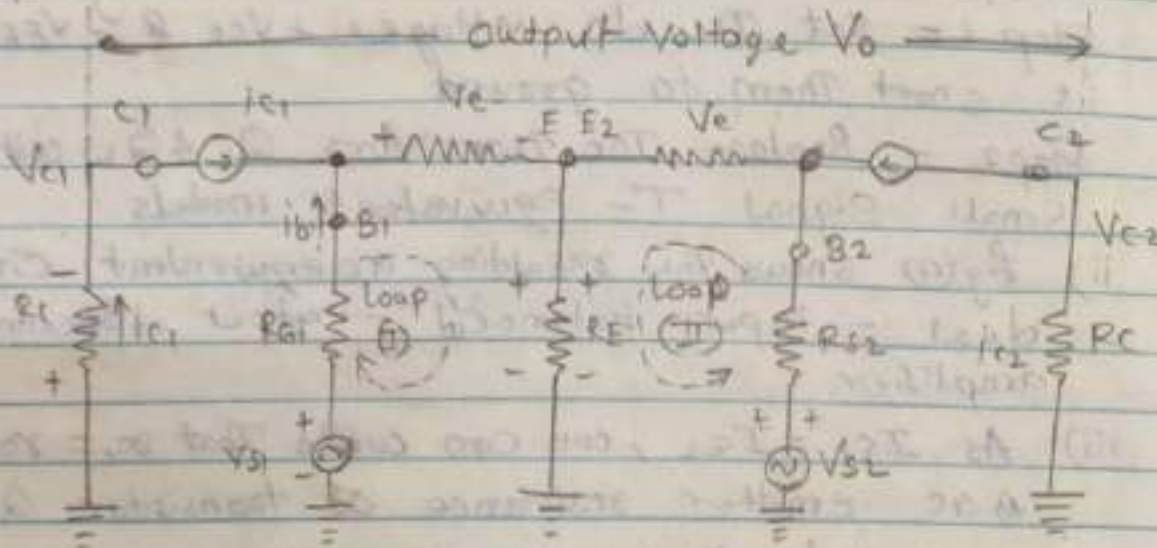
In this equation the term $V_{S1} - V_{S2}$ = differential i/p voltage V_d.

$$V_{S1} - V_{S2} = V_d$$

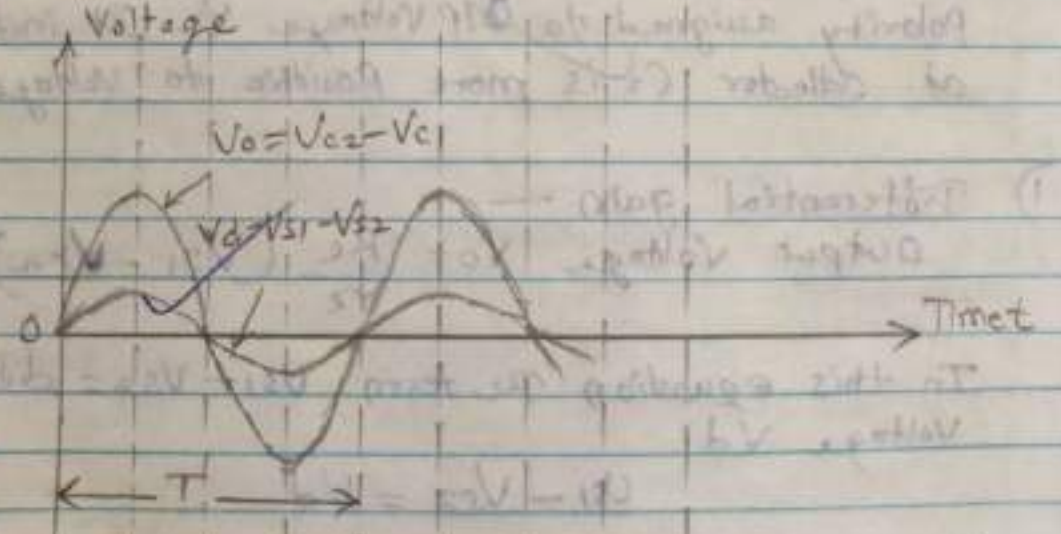
The voltage gain of dual input balanced output differential amplifier

$$A_d = \frac{V_o}{V_d} = \frac{R_c}{r_e}$$

A positive gain indicates that V_o & V_d are in phase with each other.



(a) AC equivalent circuit of dual input balanced output differential amplifier



(b) ~~Input~~ Input and output waveforms.

This expression shows that voltage gain does not depend on R_E.

Differential amplifier only the differential voltage $(V_{s1} - V_{s2})$ the i/p & o/p voltage waveform are shown in fig (b)

(2) Input Resistance (R_i) –

i) It is defined as a equivalent resistance measured at any of i/p terminals with the other terminal connected to ground

(ii) Value of R_i –

The differential i/p resistance seen from V_{s1} is given by

$$R_{i1} = \left(\frac{V_{s1}}{i_{b1}}\right)_{V_{s2}=0}$$

but $i_{b1} = i_{e1} / \beta_{ac}$

$$\therefore R_{i1} \left(\frac{V_{s1}}{i_{e1}/\beta_{ac}}\right)_{V_{s2}=0}$$

Substituting the value of i_e & $V_{s2} = 0$ we get

$$R_{i1} = \beta_{ac} \frac{[2 r_e R_E]}{R_E} = 2 \beta_{ac} r_e$$

This is the expression for R_{i1}

iii) Value of R_{i2} –

The differential i/p resistance seen from V_{s2} is given by

$$R_{i2} = \left(\frac{V_{s2}}{i_{s2}}\right)_{V_{s1}=0}$$

but $i_{b2} = i_{c2} / \beta_{ac}$

$$\therefore R_{i2} \left(\frac{V_{s2}}{i_{e2}/\beta_{ac}}\right)_{V_{s1}=0}$$

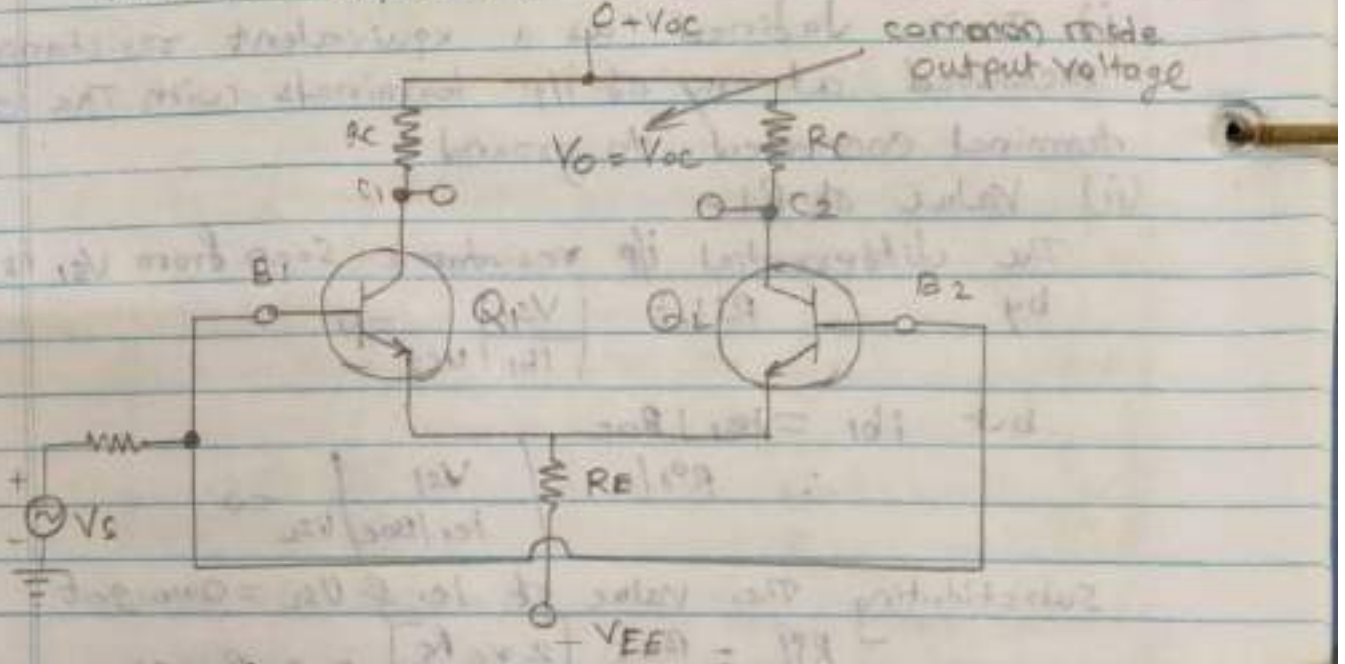
Substituting R_{i2} value of i_{e2} & $V_{s1} = 0$ we get

$$R_{i2} = \frac{\beta_{ac} r_e (r_e + 2R_E)}{(r_e + R_E)}$$

Assuming $R_E >> r_e$ we get

$$\therefore R_{i2} \doteq 2 \beta_{ac} r_e$$

This is expression for R_{i2}.



(C) Arrangement to measure the common mode gain A_d

(3) Output Resistance (R_o) —

i) o/p resistance R_o is defined as equivalent resistance measured at any of o/p terminals w.r.t. ground

ii) That means, R_{o1} is measured bet^n collector C1 to ground & R_{o2} is measured bet^n collector to C2 ground.

iii) From Fig (a) we conclude R_{o1} & R_{o2} have same value equal to R_C.

$$\therefore R_o = R_{o1} = R_{o2} = R_C$$

4) Common mode gain –

i) The common mode voltage gain can be obtained by applying a common signal i/p Vs to both i/p as shown in fig (c) & measuring the common mode o/p voltage Voc bet^n the collector of two transistor

ii) The common mode voltage gain is given by

$$Ac = \frac{Voc}{Vs}$$

Q.2 Define the characteristics of a practical op-amp

1) I/P offset voltage

2) CMRR 3) PSRR 4) slew rate

Ans: 1) I/P offset voltage –

i) A small differential i/p voltage that is required to be applied to an op-amp in order to make its o/p zero is called as i/p offset voltage.

ii) The i/p offset voltage is denoted by Vios. The i/p offset voltage is normally in a few mV range. The value of i/p offset voltage is temp. dependent. Ideally Vios should be equal to zero.

2) Common Mode Rejection Ratio (CMRR) –

i) for an op-Amp, the common mode rejection ratio is defined as the ratio of differential gain to common mode gain.

$$\therefore CMRR\ (\rho) = \frac{Ad}{Acm}$$

ii) CMRR indicate the capability of the op-Amp to successfully reject the common mode signals. CMRR is denoted by ρ if it is generally expressed in decibels (dB)

iii) CMRR should be as high as possible to reject the common mode signals such as noise successfully

3) Power Supply Rejection Ratio (PSRR) -

i) The change in an op-Amps I/P offset voltage (Vios) due to variation in the supply voltage is called as power supply rejection ratio R(PSRR)

ii) Mathematically $PSRR = \frac{\Delta V_{ios}}{\Delta V}$

Where ΔV_{ios} = change in i/p offset voltage

ΔV = Change in the supply voltage

It expressed in micro volts per volt or in decibles

(iii) The value of PSRR should ideally be equal to zero & practically it should be small as possible.

4) Slew Rate -

i) slew rate defined as maxm rate of change of o/p voltage per unit time Mathematically

$$SR = \frac{dV_o}{dt}\Big/_{max^m} \quad \text{Volts/sec}$$

(ii) The unit of slew are volts / microseconds.

Q3 Why DC level shifting is required in LIC ? Draw & explain various level shifting circuits

A) When the I/P signal passes from the one stage to the other its dc level goes on increasing Due to increased dc level output voltage gets distorted. It also limits the maxm output

Voltage swing

3) Therefore we have to use a level shifting stage to bring the dc level to zero volts w.r.t. ground

4) There are number of level shifter or translator circuits available

2) DC level shift stage using PNP-NPN transistor -

i) fig (e) shows the dc level shifter circuit using PNP- NPN transistor

ii) Voltage across R_1 i.e. $V_{R1} = V_{cc} - V_{BE1} - V_{in}$

Therefore current $I_1 = \frac{V_{R1}}{R_1} = \frac{(V_{cc} - V_{BE1} - V_{in})}{R_1}$

O/P voltage $V_{out} = I_1 \times R_2$

$$V_{out} = \frac{R_2 (V_{cc} - V_{BE1} - V_{in})}{R_1}$$

~~iii)~~

iii) By adjusting the value of R_2 it is possible to adjust the dc shift at o/p to desired value

3) level shifter using a constant current source -

i) fig (f) shows the constant current source or current mirror.

ii) The constant current source or current mirror circuit can adjust the value of I_c in such away that get zero dc voltage at the output

Q4. What is slew rate ? what are its causes ? Derive an expression for f_{max}. freq? of operation for desired o/p swing in terms of slew Rate.

Ans:- Definition :- slew rate defined as the maximum Rate of change of o/p Voltage per unit time. Mathematically it is expressed.

$$SR = \frac{dV_o}{dt}\Big|_{max} \text{ Volts/}\mu s$$

ii) The unit of slew Rate are volts/microseconds

iii) slew rate decided the capability of op-Amp to change its o/p rapidly hence it decides the highest frequency of operation of a given OP-Amp

iv) The value of slow rate depends on the change in voltage gain Therefore it is generally specified at unity gain.

v) slew rate should be ideally & Practically as high as ~~positive~~ possible.

vi) value of slew rate of an OP-Amp decides the max^m frequency (f_m) which can be amplified by the OP-Amp without introducing any distortion

$$f_m = \frac{S}{2\pi V_m}$$

where V_m = Peak i/p Voltage.

Conclude.

Unit 5

Q1. Explain with the help of circuit Diagram the operation of an OP-Amp inverting & non-inverting amplifier. Derive an expression for the voltage gain of this amplifier.

Ans:- The inverting Amplifier -

i) The circuit Diagram of an inverting amplifier is as shown in fig (a)

ii) The signal which is to be amplified is applied at the inverting (-) input terminal of OP-Amp

iii) The signal to be amplified (V_s) has been connected to inverting terminal via resistance R_1

iv) The other resistance R_F connected betn the o/p & inverting i/p terminals called as feedback resistance.

v) The non-inverting (+) input terminal is connected to ground.

vi) As the ~~inverting~~ OP-Amp is an ideal one. its open loop voltage gain $A_V = -\infty$ & i/p resistance $R_i = \infty$

vii) The o/p waveforms are shown in fig (b)

viii) From fig (a) $V_o = |A_V| \times V_d$

$$\therefore V_d = \frac{V_o}{|A_V|}$$

where A_V = open loop gain of OP-AMP

As we know A_V, of open loop is ∞

$$\therefore V_d = \frac{V_o}{\infty}$$

$\therefore V_d = 0$ But $V_d = V_1 - V_2$

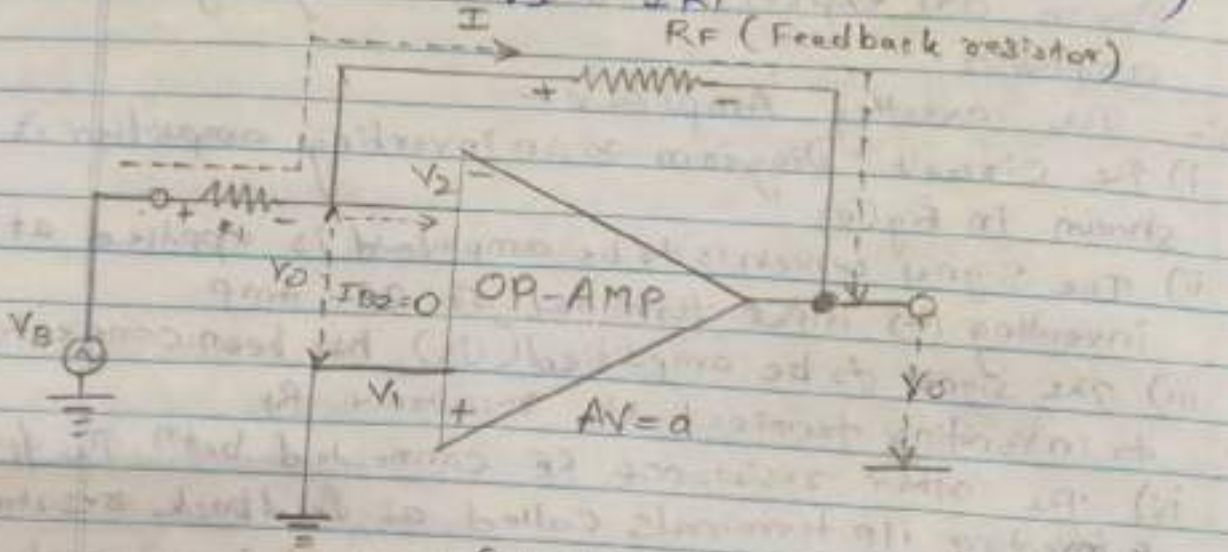
$\therefore V_1 - V_2 = 0$

Substituting ~~V_o~~ $V_1 = 0$ we get $V_2 = 0$

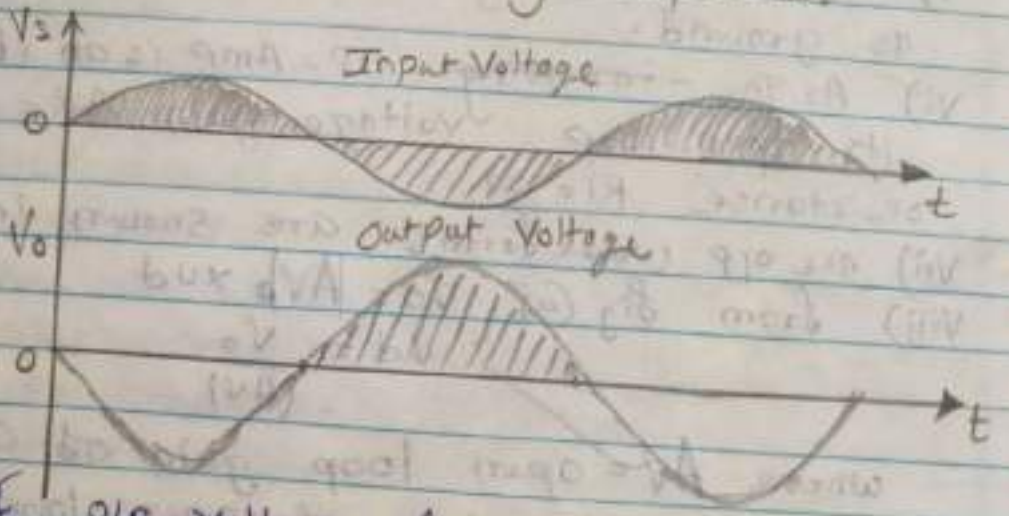
Thus V_2 is at ground potential

$R_i = \infty$ The i/p voltage is given by

$V_s = IR_1$



(a) Inverting amplifier.



∴ o/p voltage $V_o = -IR_F$

closed loop gain $A_{VF} = \frac{V_o}{V_s}$

Substituting V_o & V_s. $A_{VF} = \frac{I R_F}{I R_1}$

$= \frac{R_F}{R_1}$

& $V_o = A_{VF} \times V_s$

2) Non - inverting amplifier -

i) The non - inverting amplifier using op-Amp shown in fig (c)

ii) Here the signal which is to be amplified is applied to the non- inverting (+) input terminal of op-Amp & the inverting (-) i/p terminal is connected to ground via R_1

iii) The negative feedback is introduced in this circuit via feedback resistance RF which is connected b/w o/p & inverting (-) i/p terminal of op-Amp.

iv) As we are using an ideal op-Amp $R_i = \infty$. Therefore $I_1 = I_2 = 0$

v) Therefore voltage across R_1 by

$$V_2 = \frac{R_1}{(R_F + R_1)} V_o$$

$$V_1 = V_s - V_2$$

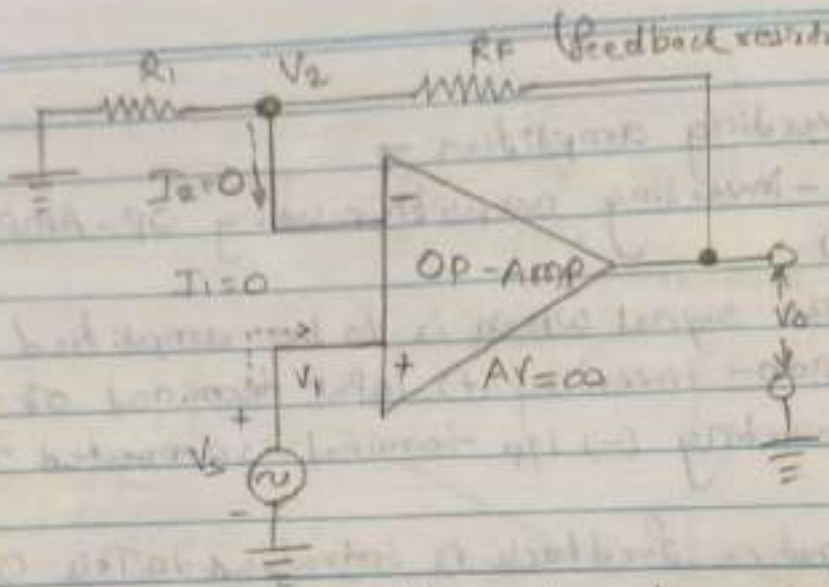
vi) Substituting expression for V_2,

$$\therefore V_s = \frac{R_1}{(R_F + R_1)} = V_o$$

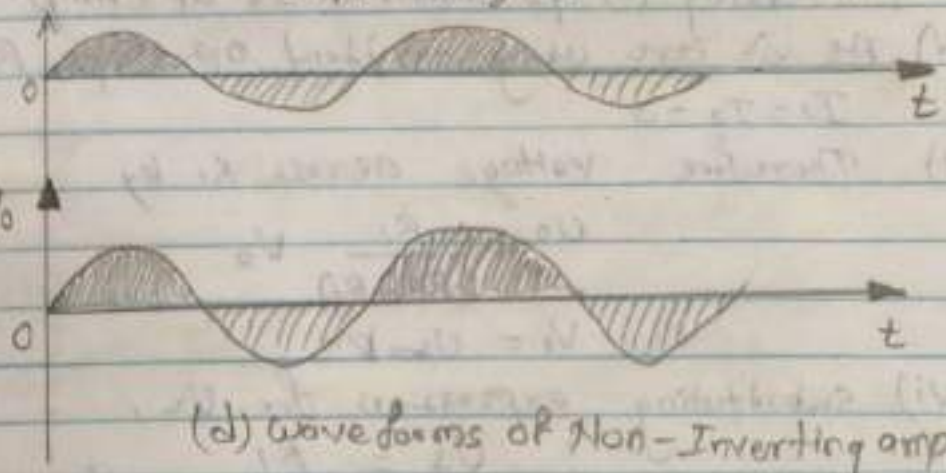
$$A_{VF} = \frac{V_o}{V_I}$$

$$= \frac{R_1 + R_F}{R_1} = 1 + \frac{R_F}{R_1}$$

& $V_o = A_{VF} \times V_S$



(c) Non-inverting amplifier



(d) Waveforms of Non-Inverting amplifier

Q2. Explain the operation of device the expression for output voltage of differential input differential output amplifier.

Ans:- (i) Differential input voltage is the maximum voltage that can be supplied to the input of pins without causing damage. The voltage is suitable as a reference for the inverting & non-inverting terminals.

ii) A differential output voltage; the difference betn the values of two AC voltages 180° out of phase present at the o/p terminal of an amplifier

when we apply differential i/p voltage to the i/p terminal of an amplifier.

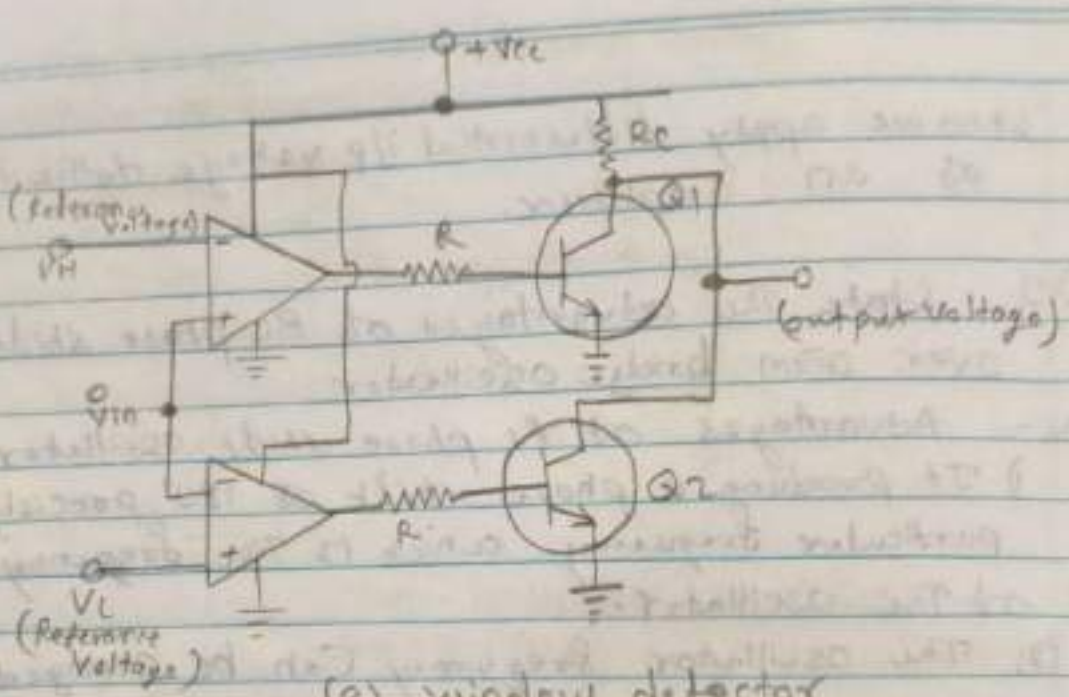
Q.3. State the advantages of Re phase shift oscillator over wien bridge oscillator

Ans:- Advantages of Re phase shift oscillator -

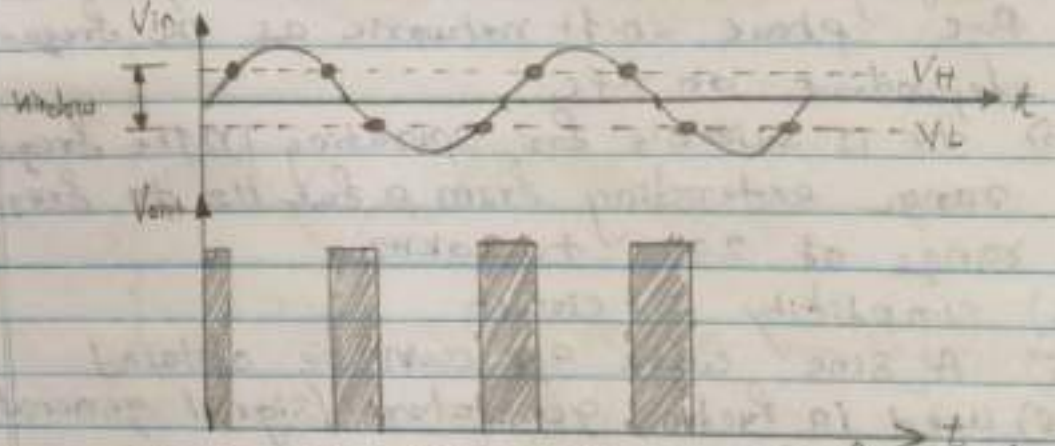
1) It produce a phase shift of 180° precisly only at the particular frequency which is the freguney of operation of the oscillator.
2) The oscillator frequency can be changed by changing either the resistors or capacitor in the R-C phase shift network as the freguency is dependant on RfC
3) It is suitable for operating in the freguency range extending from a few Hz to freguency range of 20Hz to 20KHz
4) Simplicity of circuit
5) A sine wave o/p can be obtained
6) Used in fuction generators / signal generator used in laboratoric.
7) It doesn't require any negative feedback & stabilization arrengements.

Q.4 Enlist application of comparator & explain any one of them:

Ans:- Application of Comparators



(e) window detector



Input and output voltage waveforms for a window detector

1) In signal generation & transmission
2) Automatic control & measurement.
3) A/D Converter
4) level detector & window comparator
5) V-F Converter
6) switching regulator.

Window Comparator –

i) The window detector circuit using two comparators is shown in fig (e).

ii) The window detector circuit is used for detecting whether an unknown voltage Vin falls within a specified voltage band called window.

iii) V_H & V_L are two reference voltage with $V_H > V_L$ & Vin is the input ~~The~~ voltage.

iv) If Vin is bet^n two reference voltage i.e. $V_L < V_{in} < V_H$ Then the o/p of both comparators will be low.

v) Collector voltage i.e. o/p voltage will be equal to V_{cc}.

$\therefore V_o = +V_{cc}$: For $V_L < V_{in} < V_H$.

vi) This will turn off trasistor Q_1 but saturated transistor Q_2 & the o/p voltage will be V_{CE} i.e. low.

$\therefore V_o = V_{ce} =$ low : For $V_{in} < V_L$

vii) If $V_{in} > V_H$, Then o/p of comparator, will be high & that of comparator 2 will be low.

viii) Transistor Q_1 will saturate & Q_2 will remain off the o/p voltage will V_{CE} i.e. low.

$\therefore V_o = V_{CE} =$ low : For $V_{in} > V_H$

ix) Concusion – A High voltage indicator that the i/p voltage is within the window where as a low o/p voltage indicator that i/p voltage is out window.

x) The i/p voltage waveform for a window detector are as shown in fig (f).

Conjunct

Unit 6

Q.1 Explain the basic principle of D to A converter

Ans: (i) The block diagram of DAC shown in fig (a)

(ii) The basic building blocks of DAC are - A resistance network. digitally controlled electronic switches a voltage reference & c to v converter.

iii) A digital i/p code is applied to resistive network via the digitally controlled switches.

iv) The digitally controlled switches are turned on or off by digital i/p bits.

v) The o/p current can be converted into proportional voltage with help of c to v converter.

vi) Thus we optain analog o/p voltage proportional to digital i/p code.

vii) The actual digital to analog conversion takes place within the resistive network.

Q.2 Explain the following types of errors 1) linearity error 2) offset error 3) Gain error.

Ans:- Linearity Error—

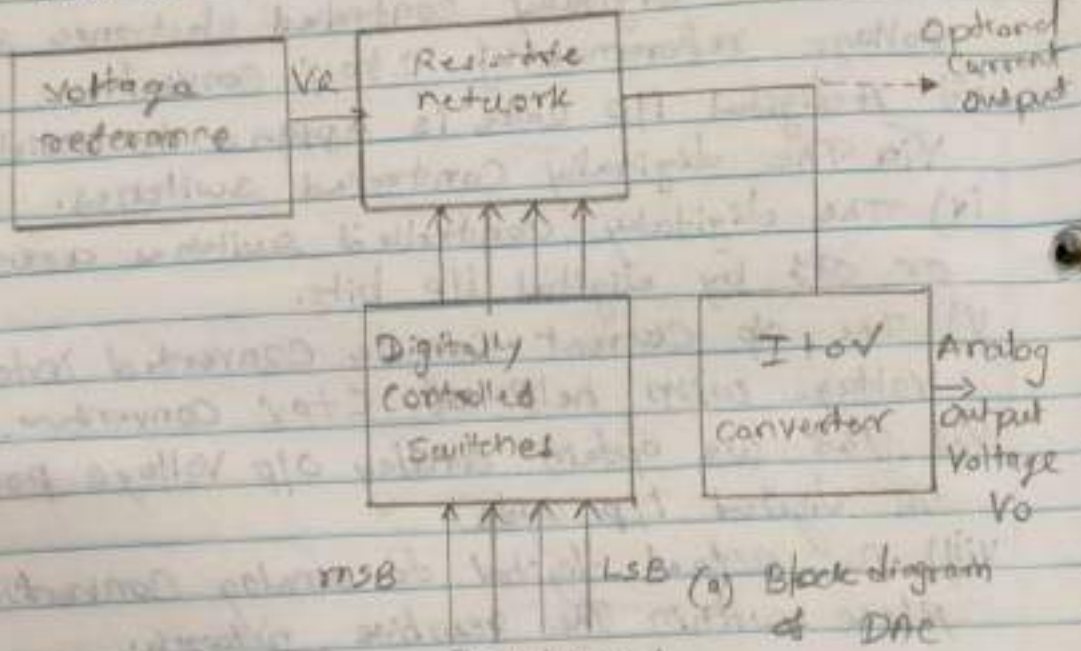
i) This is defined as the amount by which the actual o/p of a DAC differ from the ideal straight line transfer characteristics.

ii) This error is introduced due to error in the current source resistance values.

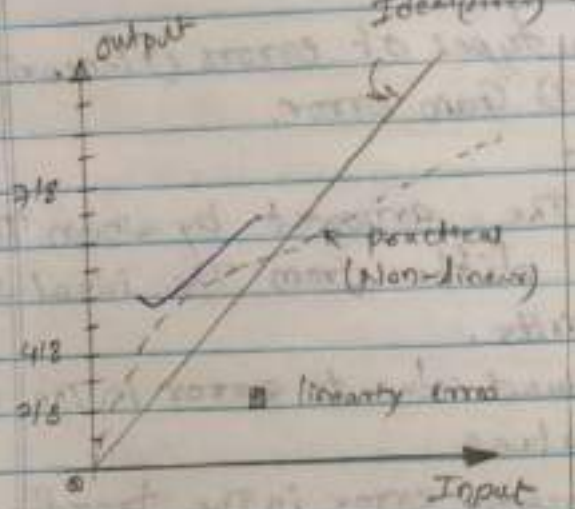
iii) fig (b) shows the linearity error in the transfer characteristics of DAC.

2) Offset Error —

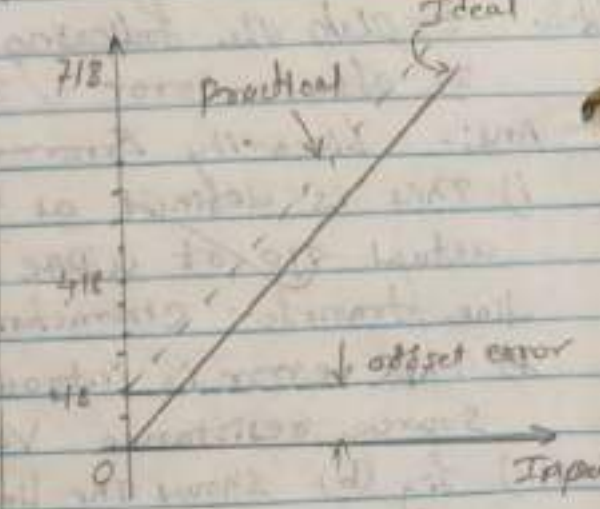
i) Ideally when all the digital i/p are 0, the analog o/p also is.



(a) Block diagram of DAC



(b) Linearity error in transfer characteristic of D/A Converter



(c) Offset error in transfer characteristics of D/A Converter

expected to be 0

ii) As shown in fig (c) same non-zero analog op voltage is present even for a zero digital i/p

iii) This called offset error. The offset error is due to the offset voltage of OP-Amp. & leakage currents in the switches

3) Gain Error –

i) In DAC we use a current to voltage converter. Therefore the analog o/p of DAC is dependent on the gain of this converter.

ii) The gain error is defined as the difference betn the theoretically calculated gain & practically obtained gain of I to V converter

iii) This error is produced due to error in feedback resistor value. The gain error is as shown in fig (d)

Q.3 What is PLL? Describe transfer characteristics of PLL. mention any four application of PLL in radio communicatn

Ans- Definition – A phase lock loop (PLL) is a control system that generates an output signal whose phase is related to phase of an i/p signal. The phase locked loop (PLL) is a closed loop system. Its application is to lock its output frequency and phase to the frequency & phase of i/p signal.

PLL Transfer Characteristics –

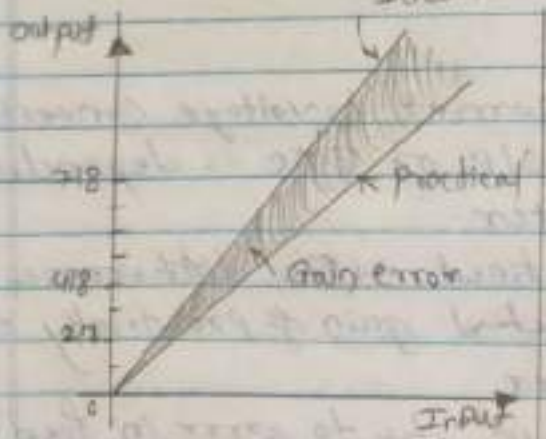
i) fig (c) shows the transfer characteristics of a PLL

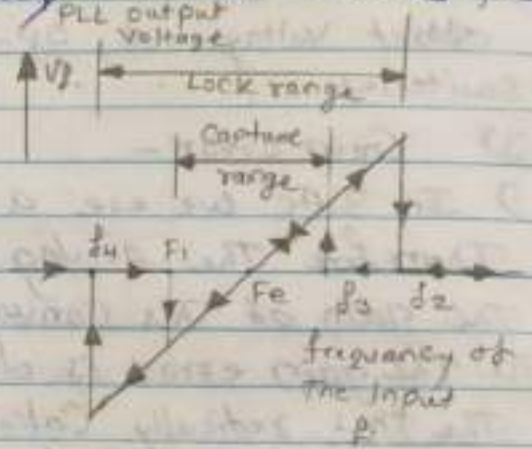
ii) It is a graph of PLL o/p voltage Vf versus the frequency of input signal i.e. fi.

iii) Transfer characteristic indicates that the PLL exhibit property of hysteresis like B-H curve.

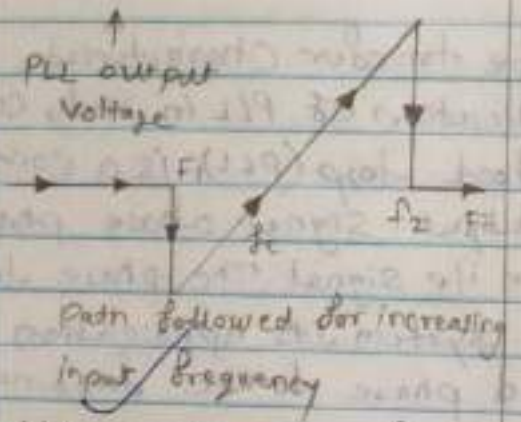
operation with increasing input frequency —

iv) Fig (f) shows that the PLL does not responds to increasing i/p frequency till it reaches the frequency f_1.



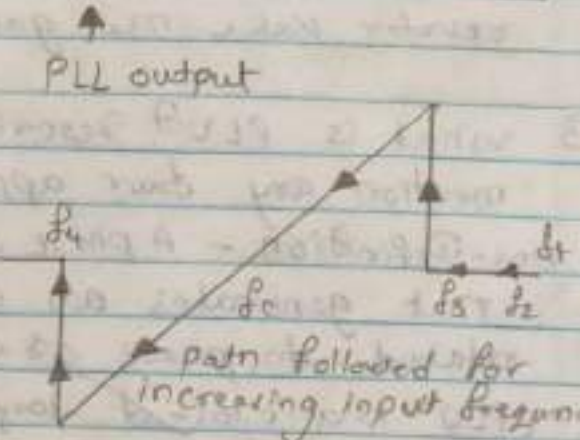


(e) transfer characteristics of a PLL



Path followed for increasing input frequency

(f) transfer curve for the increasing input frequency



path followed for increasing input frequency

(g) Transfer curve for the decreasing input frequency

v) This frequency is called as the lower edge of capture range.
vi) For increasing i/p frequency above f_1, the PLL gets locked to the input frequency.
vii) When $f_i > f_2$ i.e. the upper edge of the lock range, the PLL loosed lock, output voltage Vo reduce to 0 & VCO frequency will return to f_c.
viii) Thus the path followed for increasing input frequency is from f_1 to f_2 & then f_c as shown in fig (b)

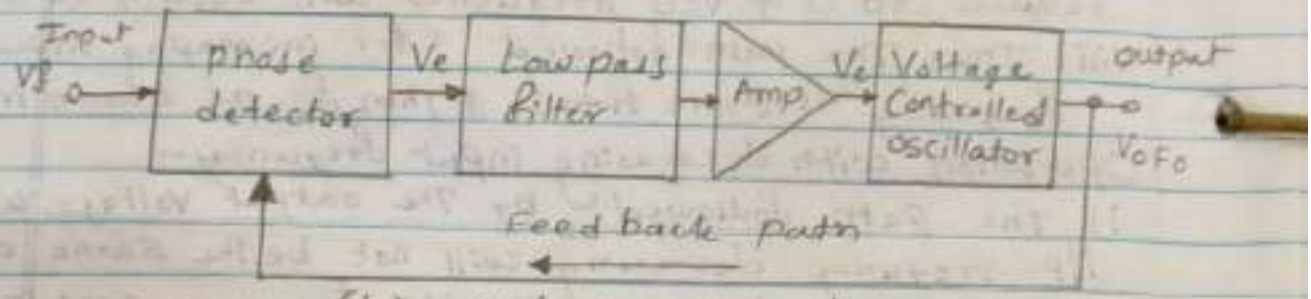
Operation with decreasing input frequency-
i) The path followed by the output voltage with the i/p frequency decreasing will not be the same as that followed when the i/p frequency was increasing.
ii) This is shown in fig (a)
iii) If the i/p frequency f_i is reduced gradually, then the PLL will recapture the signal frequency at f_3 which is called as the upper edge of capture range & tracks it upto f_4 which is the lower edge of capture range & tracks it upto f_4 which is the lower edge of the lock range.
iv) Thus from PLL transfer curve of fig (b) we can write that. $f_3 - f_1$ = capture range
$f_2 - f_4$ = lock range.

Application of PLL-
(1) Frequency multiplication division
(2) Frequency translation
(3) Amplitude demodulation
(4) Frequency demodulation
(5) tracking Filter

Q.4 Define The block diagram & transfer Curve for PLL & explain

Ans:- Block Diagram —

i) The PLL circuit is basically used for tracking a particular system



(b) A basic phase locked loop

ii) It synchronizes its o/p with The i/p signal in terms of frequency & phase.

iii) The State of synchronization bet^n The input & output is called as The locked state. In The locked state The phase error bet^n input & output is minimum.

iv) If The error tries to creep in. Then The PLL system will work automatically to minimize The phase error.

v) Thus The phase of the output signal is locked to that of The input signal. Hence The name phase locked loop.

vi) Block dia. of basic phase locked loop is as

vii) As shown in this block ~~dig~~ diagram The phase locked loop consists of:

1) A phase detector ~~of~~ or phase comparator
2) A low pass filter
3) An error amplifier
4) A voltage controlled oscillator (VCO)

Transfer characteristics —

i) Fig (e) shows the transfer characteristics of PLL.
ii) It is a graph of PLL output voltage VF (plotted on the Y-axis) versus the frequency of the input signal i.e. f_i (plotted on X-axis)
iii) The transfer characteristics indicates that the PLL ~~exi~~ exhibits the property of hysteresis like BH curve.

Conjugate.

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721657521E	Abhishek kumar yadav	9	9	8	8	9	8	8	9	68	23
72165771M	Ajay mohan gawade	9	9	9	7	9	7	7	9	64	20
71826107M	AJINKYA BALIBA KADAM	8	7	8	7	7	6	7	7	58	21
72165777L	Akash Dadaso Jadhav	8	8	7	8	8	7	8	8	62	20
72165767C	Akash Sampat Deshmukh	9	9	8	7	9	8	7	9	66	21
72029174L	Akshay Ramling Mane	8	7	8	8	9	8	8	9	67	21
721658028	Aniket dattatray sase	9	7	8	7	7	8	7	7	60	20
72165754M	Aniket Shivaji sapnar	7	7	8	7	7	8	7	7	58	20
72165755K	Ankit Gupta	7	8	8	7	8	8	7	8	61	20
72165763L	Anup H Chaudhari	8	8	8	8	8	8	8	8	64	21
72165756H	Aoudat Pravin Ravsaheb	8	8	8	8	8	8	8	8	64	20
72165760M	Arjun yashwant dinde	9	7	7	7	7	7	7	7	58	20
72165762B	Ashutosh Toundkar	9	7	7	7	7	7	7	7	58	20
72165758D	Ashwini chavhan	7	7	8	7	7	8	7	7	58	20
72165759G	Atish shankar Awaghade	8	8	7	7	9	7	7	9	63	21
719139828	Avinash Harishchandra Satale	8	8	7	8	9	7	8	9	65	22
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72165773H	Dilip Ghure	8	8	7	8	8	7	8	8	62	20
72165769K	Dixit Prashant Manikrao	8	9	8	7	9	8	7	9	65	23

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72165753C	Gade Adesh Balasaheb	7	8	7	8	8	7	8	8	63	22
721657838	Ganesh Tulshidas Kumbhar	8	9	7	8	9	7	8	9	65	23
72165772K	Ghare sagar vitthal	9	7	8	7	7	8	7	7	60	21
72165791F	Jitendra Vasant Patil	7	7	7	8	7	7	8	7	58	20
72165775D	Krishna Gupta	9	8	8	7	6	8	7	8	63	20
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72165795J	Pawar Dadasaheb Nanasaheb	9	9	8	7	9	8	7	9	65	21

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72165813L	Prathamesh dipak vichare	9	9	9	9	9	9	9	9	72	23
72165805K	Pratik Shinkar	8	9	8	9	9	9	9	9	70	23
72165758G	Priyanka ramesh suryawanshi	8	8	9	9	9	9	9	9	70	23
72165797E	Rahul B. Kamtikar	9	9	9	9	9	9	9	9	72	23
71913948B	Rajkumar balasaheb dalvndkar	8	9	8	9	9	9	9	9	70	23
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72165788F	Rushikesh Fulchand Palkar	9	9	9	9	9	9	9	9	72	23
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72165766E	Ruturaj Deshmukh	9	9	9	9	9	9	9	9	72	23
72165782G	Sadhana shantling kshirsagar	9	9	9	9	9	9	9	9	72	23
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72165800J	Saiprasad Nandkumar Shinde	9	9	9	9	9	9	9	9	72	23
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72165801G	Santosh Sarjerao Gade	9	9	9	9	9	9	9	9	72	23
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72165804M	shahil pawar	9	9	9	9	9	9	9	9	72	23
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72165790H	vivek Pandey	9	9	9	9	9	9	9	9	72	23
72165815G	Yasin Ramjan Mujawar	9	9	9	9	9	9	9	9	72	23

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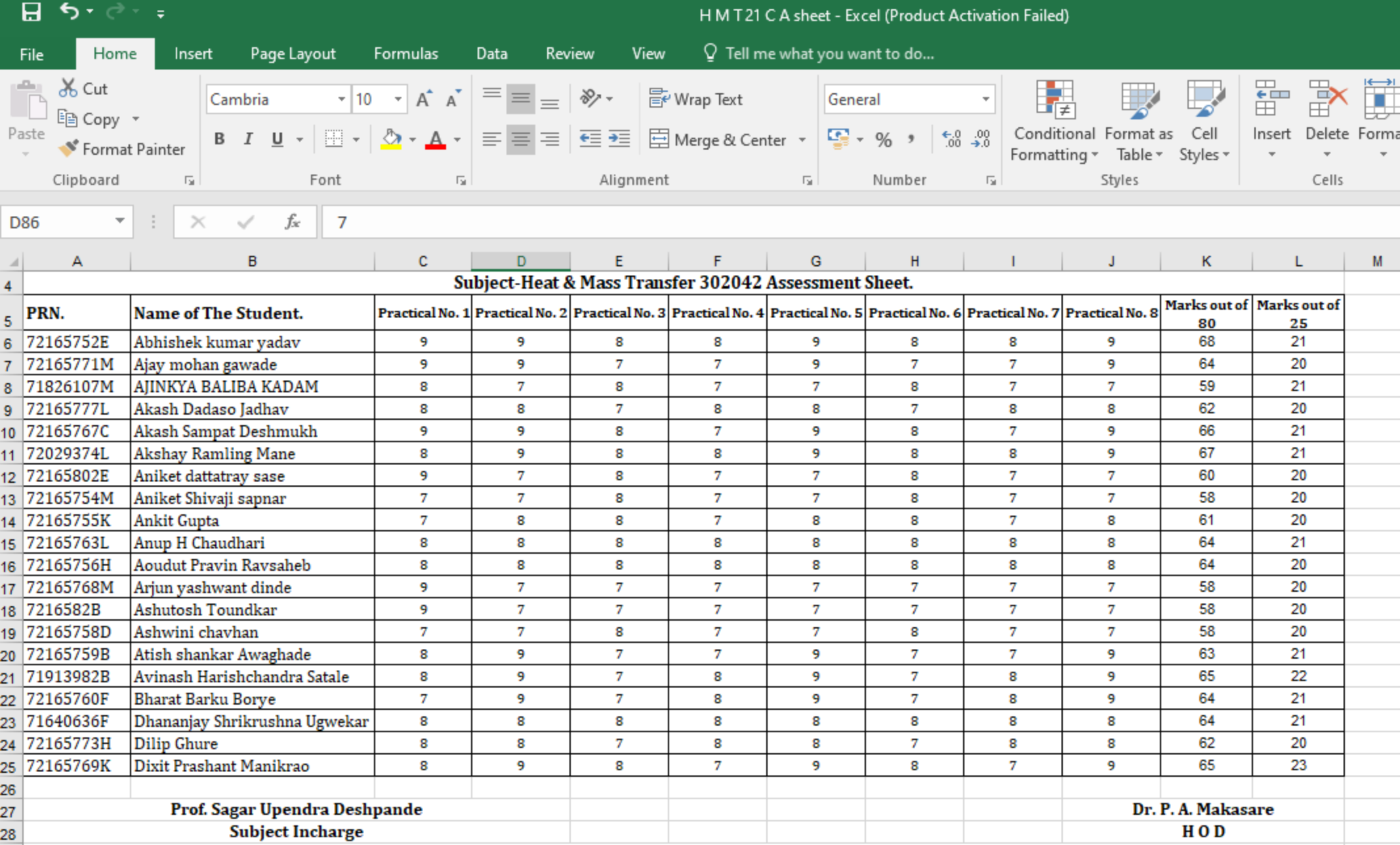

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Lecture count for Slow-Learner AY 2021-22. Sem I & II

YEAR	DEPT	Sr. NO.	SUBJECT	LECTURE COUNT
FE	FE	1	1) Engineering Mathematics -I	9
		2	2) Engineering Mechanics -I	10
SE	MECH	1	Solid of Materials	9
		2	Electrical & Electronics Engg.	8
		3	Engineering Mathematics -III	10
SE	CIVIL	1	Mechanics of Structure	9
		2	Fluid Mechanics	10
		3	Engineering Mathematics -III	10
SE	E&TC	1	Data Structures	8
		2	Signals & Systems	10
		3	Engineering Mathematics -III	10
SE	COMP	1	Microprocessor	9
		2	Engineering Mathematics -III	10
SE	IT	1	Processor Architecture & Interfacing	9
		2	Engineering Mathematics -III	10

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